Aurelii Communications

Preliminary Data Sheet

Gold Code Generator Peripheral

Features:

- 5 bit Fibonacci Linear Feedback Shift Registers
- Fixed 5 bit Register Contents for Pseudorandom (PN) Sequence 0
- Variable 5 bit Register Contents for Pseudorandom (PN) Sequence 1
- 16 Channel Serial Gold Code Output
- Global Output Enable for all Gold Code Channels
- Local Output Enable for all Gold Code Channels
- Global Enable for all Gold Code Channels
- Local Enable for all Gold Code Channels
- 5 bit Address and 16 bit Microprocessor Interface
    - 4 bit PN Sequence 1 Initial Contents
    - 4 bit Control and Status Register
    - 5 bit PN 0 Readback
    - 5 bit PN 1 Readback
    - Global Enable
    - Global Output Enable
- 16 bit Output for FIFO Interface
    - 5 bit PN Sequence 0 Registers
    - 5 bit PN Sequence 1 Registers
    - 5 bit Gold Code Registers
    - 1 bit Gold Code Output

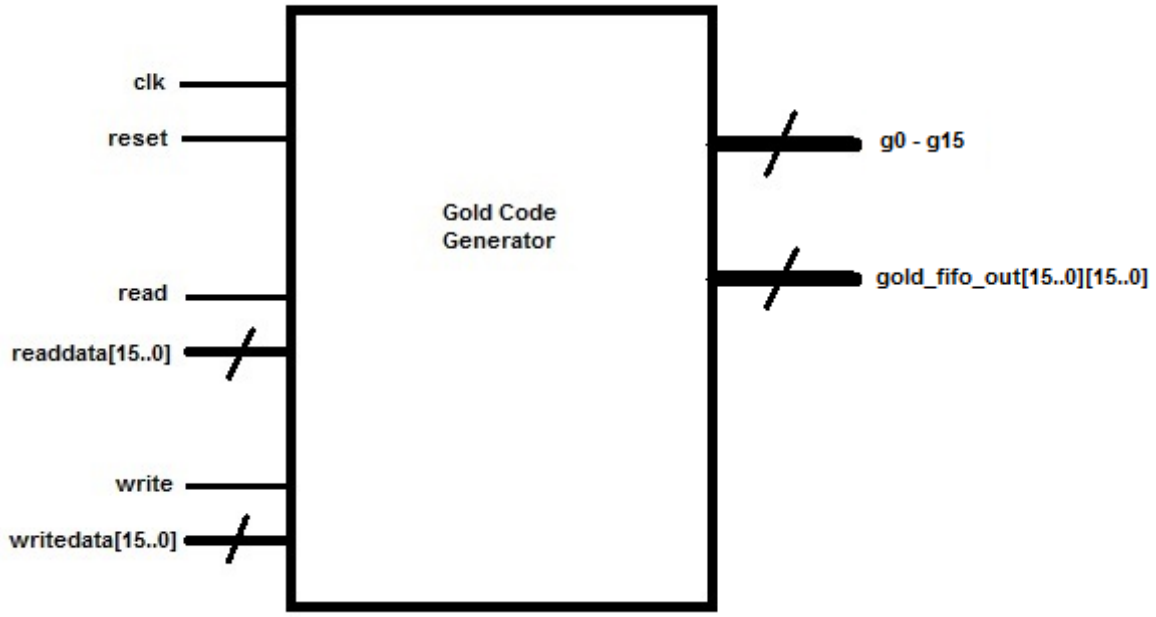

Figure 1: Gold Code Generator Block Diagram

Introduction

Gold Codes are flexible code types used for a variety of secure communication methods. The most widely used application of Gold Codes is Spread Spectrum (SS) communications. This includes both methods of Direct Sequence (DS) SS and Frequency Hopping (FH) SS modulation. Code Division Multiple Access is a method of allocating a range of the communications spectrum to a specific number of communication channels using DSSS or FHSS. The uses of Gold Codes extend far beyond Spread Spectrum communications to a variety of applications in Voice, Video, and Data transmission over a wide range of communication channel types.

Gold Code Waveforms

Figure 2 shows the output waveforms for the 16 channel serial output of the Gold Code Peripheral. The channels labeled g1 – g16 shown in Figure 2 correspond to the ports labeled g0 – g15 on the peripheral block diagram of Figure 1. Each channel contains a register that can be accessed through the microprocessor interface. This allows the user to create 16 unique codes; 1 for each channel. The clock waveform shown in the simulation is the chip clock.

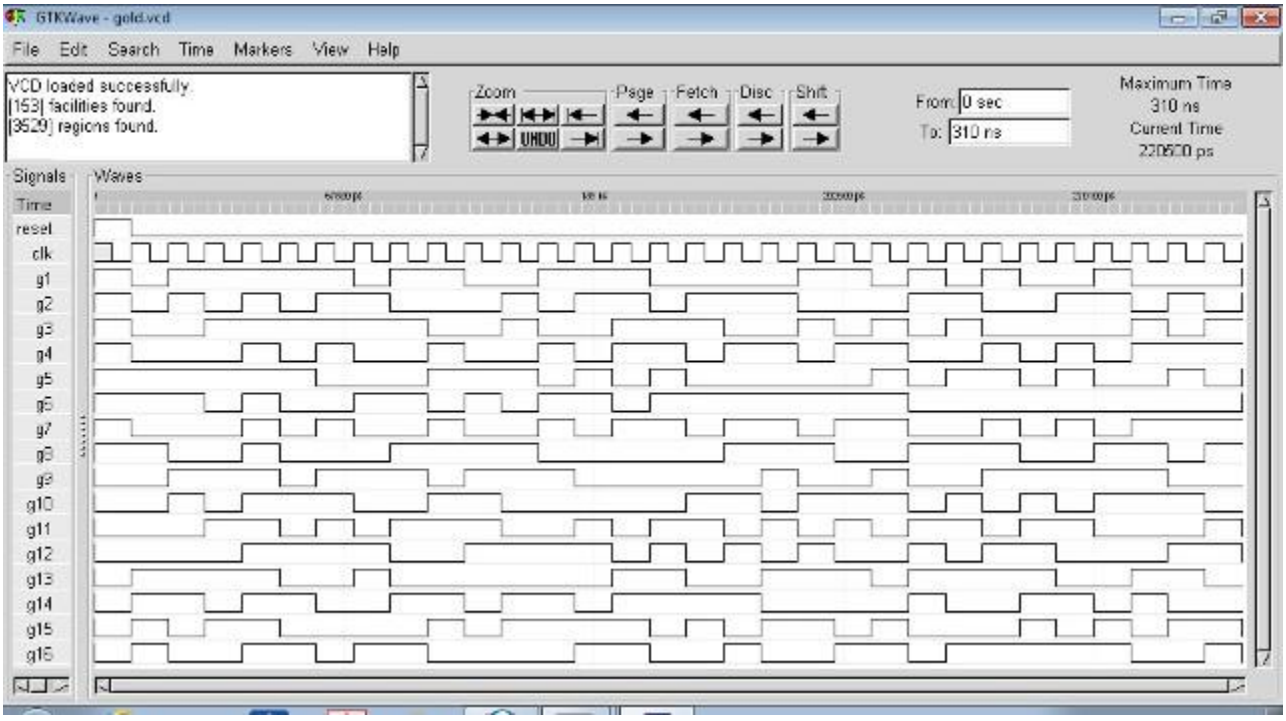

Figure 2: Gold Code Peripherial Output Waveforms (16 Channels – 5 Bit LFSR)

Microprocessor Interface

The 7 ports of the microprocessor interface for the Gold Code Peripheral are shown below.

reset	-	Peripheral reset
clk	-	Chip Clock
address	-	5 bit address (bits 4 down to 0) for accessing peripheral registers
write	-	Register write enable
writedata	-	16 bit write data (bits 15 down to 0) for peripheral registers
read	-	Register read enable
readdata	-	16 bit read data (bits 15 down to 0) for peripheral registers

Writing to the peripheral registers requires

1) The write address be present on address[4:0]
2) The write data be present on writedata[15:0]
3) The write enable be asserted

Reading from the peripheral registers requires

1) The read address be present on address[4:0]
2) The read data be present on readdata[15:0]
3) The read enable be asserted

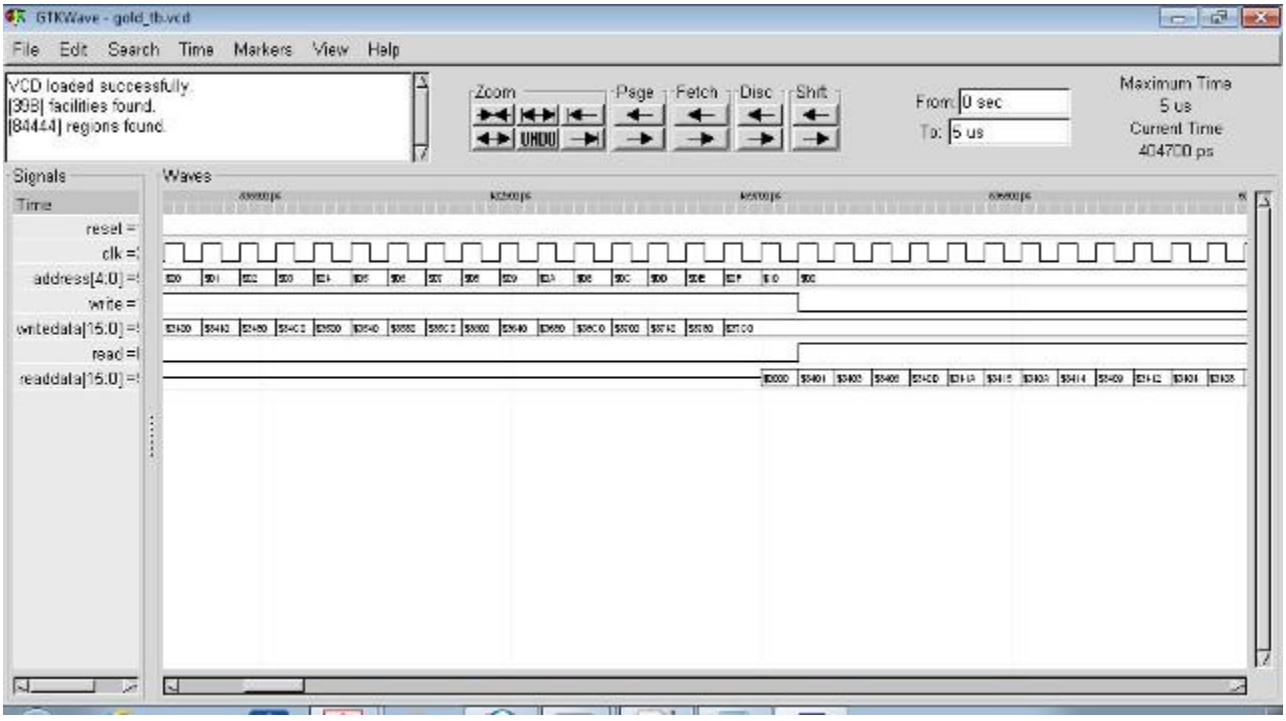

Figure 3: Microprocessor Interface with Read/Write illustrations

Clock Enable

Each Gold Code channel can be enabled individually or as a group. The control and status register (CSR) of each Gold Code channel has a bit that controls the enable of that channel. There is also an enable that controls all 16 Gold Code channels. The default setting for both the individual enable and the enable that controls all 16 channels is disabled. The user can set the individual enables and then set the enable that controls all 16 channels to enable the Gold Code channels as a group. The user can also set the enable that controls all 16 channels and then set the enable that controls the individual channels to enable each individual channel respectively.

The simulation in Figure 4 shows the Gold Codes channels being enabled as a group.

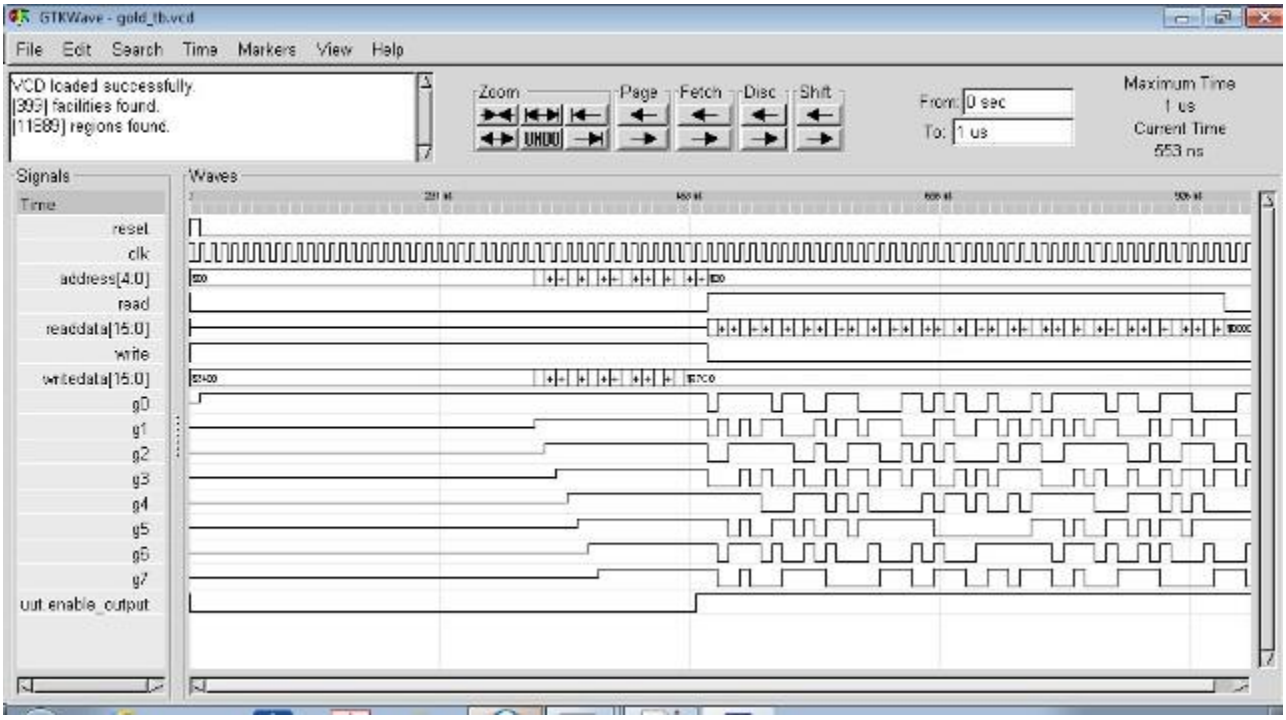

Figure 4: Gold Codes being enabled as a group and tri stated individually

Output Enable

Each Gold Code channel pin can be tri stated individually or as a group. The control and status register (CSR) of each Gold Code channel has a bit that controls the output enable of that channel. There is also an output enable that controls the output of all 16 Gold Code channels. The default setting for both the individual output enable and the output enable that controls all 16 channels is disabled. The user can set the individual output enables and then set the output enable that controls all 16 channels to tri state the Gold Code channels as a group. The user can also set the output enable that controls all 16 channels and then set the output enable that controls the individual channels to tri state each individual channel respectively.

The simulation in Figure 4 shows the Gold Codes channels being tri-stated individually. The simulation in Figure 5 shows the Gold Code channels being tri-stated as a group.

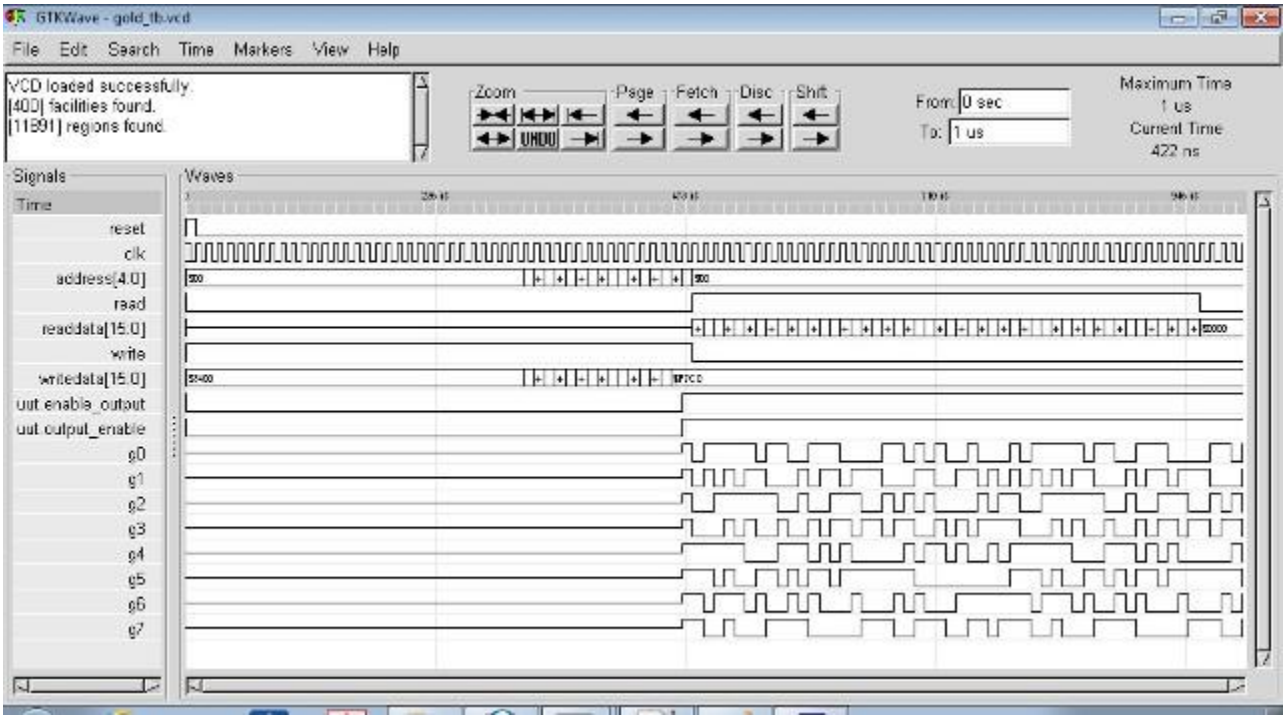

Figure 5: Gold Code channels being tri stated as a group

First In First Out (FIFO) Interface

The Gold Code Module has a 16 bit Output FIFO interface. The FIFO interface can be connected to the input of a FIFO. The bits are organized as shown below:

[15]	Gold Code Output Register
[14..10]	Gold Code Registers
[9..5]	PN 1 Registers
[4..0]	PN 0 Registers

This allows the user to examine the contents of the Gold Code generator while the Gold Code channel output is running.

The output of the FIFO may be used to interface to a Direct Memory Access (DMA) Controller.

Figure 6 shows the parallel FIFO output interface for a single channel. Figure 7 shows the parallel FIFO outputs for all 16 channels.

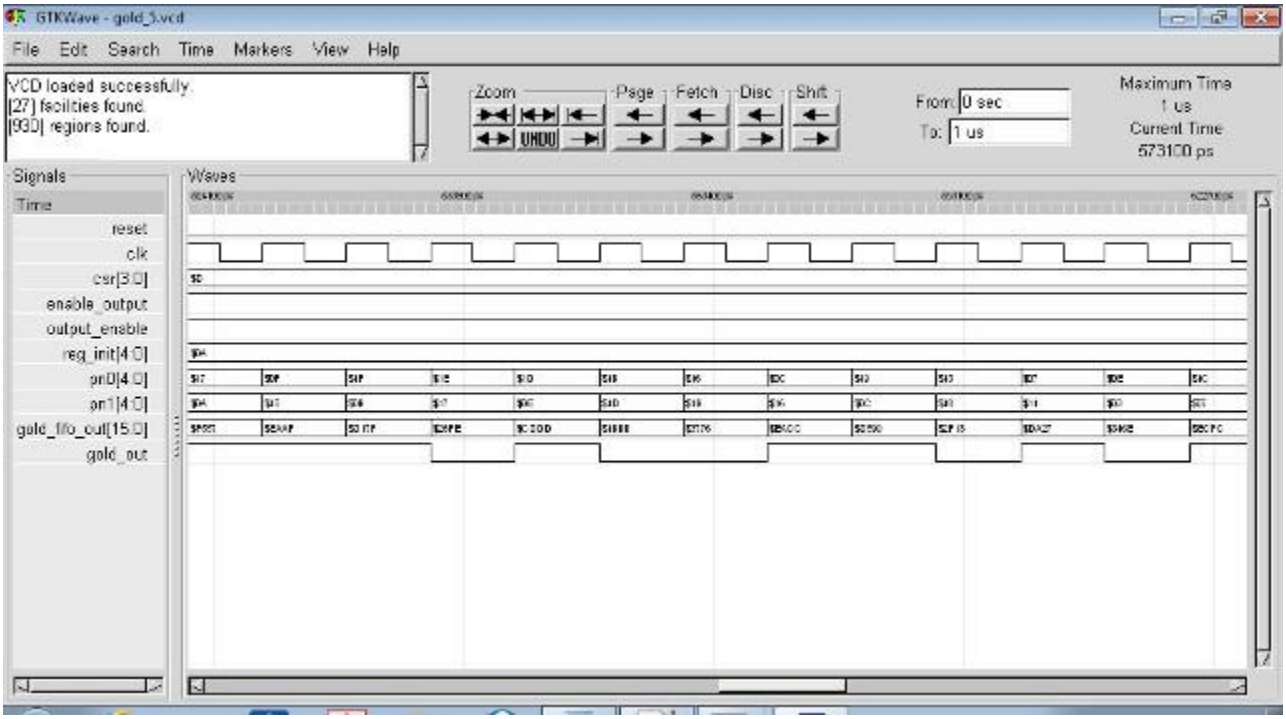

Figure 6: Parallel FIFO Interface – Single Channel

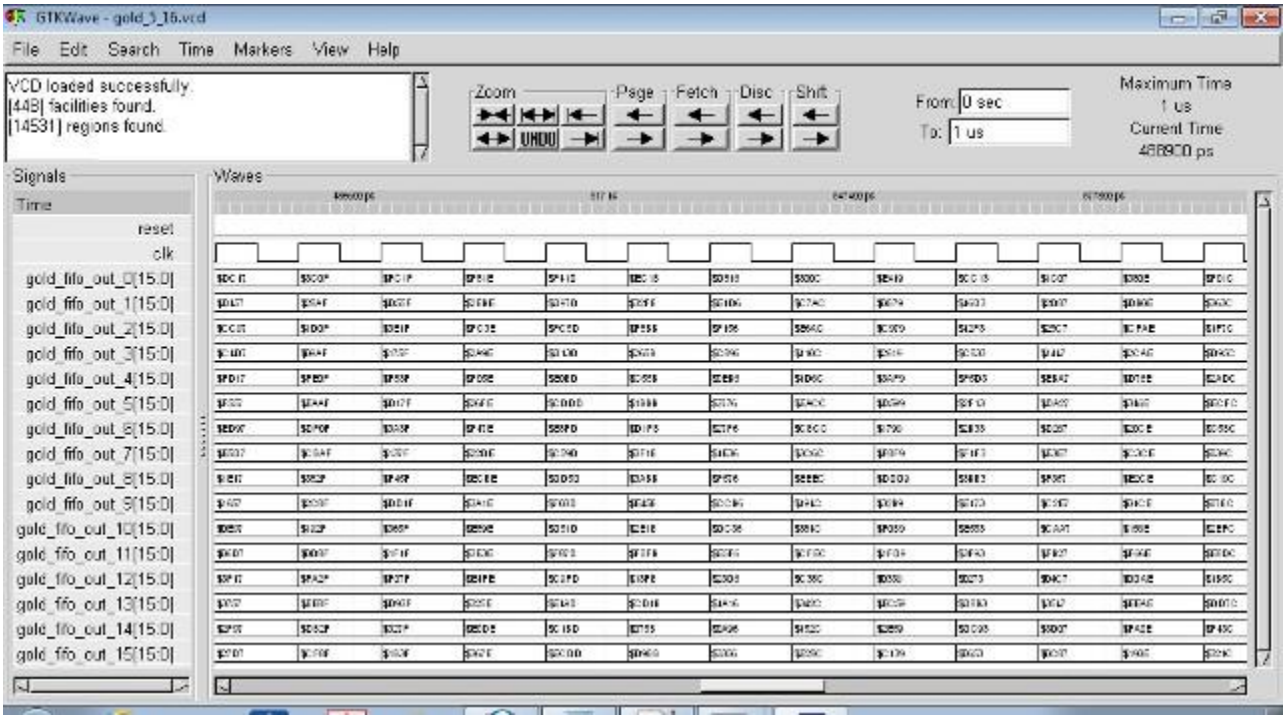

Figure 7: 16 Channel 16 bit Gold Code Output FIFO Interface

Port Declarations

Port	Width	Description
CLK	1	Chip Clock
RESET	1	Peripheral Reset
READ	1	Read Enable
READDATA	16	Read Data
WRITE	1	Write Enable
WRITEDATA	16	Write Data
GOLD_FIFO_OUT_0	16	Channel 0 FIFO Output
GOLD_FIFO_OUT_1	16	Channel 1 FIFO Output
GOLD_FIFO_OUT_2	16	Channel 2 FIFO Output
GOLD_FIFO_OUT_3	16	Channel 3 FIFO Output
GOLD_FIFO_OUT_4	16	Channel 4 FIFO Output
GOLD_FIFO_OUT_5	16	Channel 5 FIFO Output
GOLD_FIFO_OUT_6	16	Channel 6 FIFO Output
GOLD_FIFO_OUT_7	16	Channel 7 FIFO Output
GOLD_FIFO_OUT_8	16	Channel 8 FIFO Output
GOLD_FIFO_OUT_9	16	Channel 9 FIFO Output
GOLD_FIFO_OUT_10	16	Channel 10 FIFO Output
GOLD_FIFO_OUT_11	16	Channel 11 FIFO Output
GOLD_FIFO_OUT_12	16	Channel 12 FIFO Output
GOLD_FIFO_OUT_13	16	Channel 13 FIFO Output
GOLD_FIFO_OUT_14	16	Channel 14 FIFO Output
GOLD_FIFO_OUT_15	16	Channel 15 FIFO Output
G0	1	Channel 0 Gold Code Output
G1	1	Channel 1 Gold Code Output
G2	1	Channel 2 Gold Code Output
G3	1	Channel 3 Gold Code Output
G4	1	Channel 4 Gold Code Output
G5	1	Channel 5 Gold Code Output
G6	1	Channel 6 Gold Code Output
G7	1	Channel 7 Gold Code Output
G8	1	Channel 8 Gold Code Output
G9	1	Channel 9 Gold Code Output
G10	1	Channel 10 Gold Code Output
G11	1	Channel 11 Gold Code Output
G12	1	Channel 12 Gold Code Output
G13	1	Channel 13 Gold Code Output
G14	1	Channel 14 Gold Code Output
G15	1	Channel 15 Gold Code Output

Table 1: Peripheral Port Descriptions

Address Tables

Register Address Map (Write)																	
Address / Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	Unused	Unused	CSR[0][3]	CSR[0][2]	CSR[0][1]	CSR[0][0]	PN1[0][4]	PN1[0][3]	PN1[0][2]	PN1[0][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x1	Unused	Unused	CSR[1][3]	CSR[1][2]	CSR[1][1]	CSR[1][0]	PN1[1][4]	PN1[1][3]	PN1[1][2]	PN1[1][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x2	Unused	Unused	CSR[2][3]	CSR[2][2]	CSR[2][1]	CSR[2][0]	PN1[2][4]	PN1[2][3]	PN1[2][2]	PN1[2][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x3	Unused	Unused	CSR[3][3]	CSR[3][2]	CSR[3][1]	CSR[3][0]	PN1[3][4]	PN1[3][3]	PN1[3][2]	PN1[3][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x4	Unused	Unused	CSR[4][3]	CSR[4][2]	CSR[4][1]	CSR[4][0]	PN1[4][4]	PN1[4][3]	PN1[4][2]	PN1[4][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x5	Unused	Unused	CSR[5][3]	CSR[5][2]	CSR[5][1]	CSR[5][0]	PN1[5][4]	PN1[5][3]	PN1[5][2]	PN1[5][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x6	Unused	Unused	CSR[6][3]	CSR[6][2]	CSR[6][1]	CSR[6][0]	PN1[6][4]	PN1[6][3]	PN1[6][2]	PN1[6][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x7	Unused	Unused	CSR[7][3]	CSR[7][2]	CSR[7][1]	CSR[7][0]	PN1[7][4]	PN1[7][3]	PN1[7][2]	PN1[7][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x8	Unused	Unused	CSR[8][3]	CSR[8][2]	CSR[8][1]	CSR[8][0]	PN1[8][4]	PN1[8][3]	PN1[8][2]	PN1[8][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x9	Unused	Unused	CSR[9][3]	CSR[9][2]	CSR[9][1]	CSR[9][0]	PN1[9][4]	PN1[9][3]	PN1[9][2]	PN1[9][1]	Unused	Unused	Unused	Unused	Unused	Unused
0xA	Unused	Unused	CSR[10][3]	CSR[10][2]	CSR[10][1]	CSR[10][0]	PN1[10][4]	PN1[10][3]	PN1[10][2]	PN1[10][1]	Unused	Unused	Unused	Unused	Unused	Unused
0xB	Unused	Unused	CSR[11][3]	CSR[11][2]	CSR[11][1]	CSR[11][0]	PN1[11][4]	PN1[11][3]	PN1[11][2]	PN1[11][1]	Unused	Unused	Unused	Unused	Unused	Unused
0xC	Unused	Unused	CSR[12][3]	CSR[12][2]	CSR[12][1]	CSR[12][0]	PN1[12][4]	PN1[12][3]	PN1[12][2]	PN1[12][1]	Unused	Unused	Unused	Unused	Unused	Unused
0xD	Unused	Unused	CSR[13][3]	CSR[13][2]	CSR[13][1]	CSR[13][0]	PN1[13][4]	PN1[13][3]	PN1[13][2]	PN1[13][1]	Unused	Unused	Unused	Unused	Unused	Unused
0xE	Unused	Unused	CSR[14][3]	CSR[14][2]	CSR[14][1]	CSR[14][0]	PN1[14][4]	PN1[14][3]	PN1[14][2]	PN1[14][1]	Unused	Unused	Unused	Unused	Unused	Unused
0xF	Unused	Unused	CSR[15][3]	CSR[15][2]	CSR[15][1]	CSR[15][0]	PN1[15][4]	PN1[15][3]	PN1[15][2]	PN1[15][1]	Unused	Unused	Unused	Unused	Unused	Unused
0x10	OE	CE	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

Table 2: Register Address Map for Write Transfers

Register Address Map (Read)																
Address / Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	Unused	Unused	CSR[0][3]	CSR[0][2]	CSR[0][1]	CSR[0][0]	PN1[0][4]	PN1[0][3]	PN1[0][2]	PN1[0][1]	PN1[0][0]	PN0[0][4]	PN0[0][3]	PN0[0][2]	PN0[0][1]	PN0[0][0]
0x1	Unused	Unused	CSR[1][3]	CSR[1][2]	CSR[1][1]	CSR[1][0]	PN1[1][4]	PN1[1][3]	PN1[1][2]	PN1[1][1]	PN1[1][0]	PN0[1][4]	PN0[1][3]	PN0[1][2]	PN0[1][1]	PN0[1][0]
0x2	Unused	Unused	CSR[2][3]	CSR[2][2]	CSR[2][1]	CSR[2][0]	PN1[2][4]	PN1[2][3]	PN1[2][2]	PN1[2][1]	PN1[2][0]	PN0[2][4]	PN0[2][3]	PN0[2][2]	PN0[2][1]	PN0[2][0]
0x3	Unused	Unused	CSR[3][3]	CSR[3][2]	CSR[3][1]	CSR[3][0]	PN1[3][4]	PN1[3][3]	PN1[3][2]	PN1[3][1]	PN1[3][0]	PN0[3][4]	PN0[3][3]	PN0[3][2]	PN0[3][1]	PN0[3][0]
0x4	Unused	Unused	CSR[4][3]	CSR[4][2]	CSR[4][1]	CSR[4][0]	PN1[4][4]	PN1[4][3]	PN1[4][2]	PN1[4][1]	PN1[4][0]	PN0[4][4]	PN0[4][3]	PN0[4][2]	PN0[4][1]	PN0[4][0]
0x5	Unused	Unused	CSR[5][3]	CSR[5][2]	CSR[5][1]	CSR[5][0]	PN1[5][4]	PN1[5][3]	PN1[5][2]	PN1[5][1]	PN1[5][0]	PN0[5][4]	PN0[5][3]	PN0[5][2]	PN0[5][1]	PN0[5][0]
0x6	Unused	Unused	CSR[6][3]	CSR[6][2]	CSR[6][1]	CSR[6][0]	PN1[6][4]	PN1[6][3]	PN1[6][2]	PN1[6][1]	PN1[6][0]	PN0[6][4]	PN0[6][3]	PN0[6][2]	PN0[6][1]	PN0[6][0]
0x7	Unused	Unused	CSR[7][3]	CSR[7][2]	CSR[7][1]	CSR[7][0]	PN1[7][4]	PN1[7][3]	PN1[7][2]	PN1[7][1]	PN1[7][0]	PN0[7][4]	PN0[7][3]	PN0[7][2]	PN0[7][1]	PN0[7][0]
0x8	Unused	Unused	CSR[8][3]	CSR[8][2]	CSR[8][1]	CSR[8][0]	PN1[8][4]	PN1[8][3]	PN1[8][2]	PN1[8][1]	PN1[8][0]	PN0[8][4]	PN0[8][3]	PN0[8][2]	PN0[8][1]	PN0[8][0]
0x9	Unused	Unused	CSR[9][3]	CSR[9][2]	CSR[9][1]	CSR[9][0]	PN1[9][4]	PN1[9][3]	PN1[9][2]	PN1[9][1]	PN1[9][0]	PN0[9][4]	PN0[9][3]	PN0[9][2]	PN0[9][1]	PN0[9][0]
0xA	Unused	Unused	CSR[10][3]	CSR[10][2]	CSR[10][1]	CSR[10][0]	PN1[10][4]	PN1[10][3]	PN1[10][2]	PN1[10][1]	PN1[10][0]	PN0[10][4]	PN0[10][3]	PN0[10][2]	PN0[10][1]	PN0[10][0]
0xB	Unused	Unused	CSR[11][3]	CSR[11][2]	CSR[11][1]	CSR[11][0]	PN1[11][4]	PN1[11][3]	PN1[11][2]	PN1[11][1]	PN1[11][0]	PN0[11][4]	PN0[11][3]	PN0[11][2]	PN0[11][1]	PN0[11][0]
0xC	Unused	Unused	CSR[12][3]	CSR[12][2]	CSR[12][1]	CSR[12][0]	PN1[12][4]	PN1[12][3]	PN1[12][2]	PN1[12][1]	PN1[12][0]	PN0[12][4]	PN0[12][3]	PN0[12][2]	PN0[12][1]	PN0[12][0]
0xD	Unused	Unused	CSR[13][3]	CSR[13][2]	CSR[13][1]	CSR[13][0]	PN1[13][4]	PN1[13][3]	PN1[13][2]	PN1[13][1]	PN1[13][0]	PN0[13][4]	PN0[13][3]	PN0[13][2]	PN0[13][1]	PN0[13][0]
0xE	Unused	Unused	CSR[14][3]	CSR[14][2]	CSR[14][1]	CSR[14][0]	PN1[14][4]	PN1[14][3]	PN1[14][2]	PN1[14][1]	PN1[14][0]	PN0[14][4]	PN0[14][3]	PN0[14][2]	PN0[14][1]	PN0[14][0]
0xF	Unused	Unused	CSR[15][3]	CSR[15][2]	CSR[15][1]	CSR[15][0]	PN1[15][4]	PN1[15][3]	PN1[15][2]	PN1[15][1]	PN1[15][0]	PN0[15][4]	PN0[15][3]	PN0[15][2]	PN0[15][1]	PN0[15][0]
0x10	OE	CE	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

Table 3: Register Address Map for Read Transfers

Register Definitions - Control and Status Registers

CSR[15:0][3:0] - 16 Channel 4 Bit Control and Status Register

CSR[0][3] - Channel 0 Bit 3 (Channel 0 Output Enable)
CSR[0][2] - Channel 0 Bit 2 (Channel 0 Channel Enable)
CSR[0][1] - Channel 0 Bit 1 (Channel 0 Synchronous Reset)
CSR[0][0] - Channel 0 Bit 0 (Channel 0 Clock Enable)

CSR[1][3] - Channel 1 Bit 3 (Channel 1 Output Enable)
CSR[1][2] - Channel 1 Bit 2 (Channel 1 Channel Enable)
CSR[1][1] - Channel 1 Bit 1 (Channel 1 Synchronous Reset)
CSR[1][0] - Channel 1 Bit 0 (Channel 1 Clock Enable)

CSR[2][3] - Channel 2 Bit 3 (Channel 2 Output Enable)
CSR[2][2] - Channel 2 Bit 2 (Channel 2 Channel Enable)
CSR[2][1] - Channel 2 Bit 1 (Channel 2 Synchronous Reset)
CSR[2][0] - Channel 2 Bit 0 (Channel 2 Clock Enable)

CSR[3][3] - Channel 3 Bit 3 (Channel 3 Output Enable)
CSR[3][2] - Channel 3 Bit 2 (Channel 3 Channel Enable)
CSR[3][1] - Channel 3 Bit 1 (Channel 3 Synchronous Reset)
CSR[3][0] - Channel 3 Bit 0 (Channel 3 Clock Enable)

CSR[4][3] - Channel 4 Bit 3 (Channel 4 Output Enable)
CSR[4][2] - Channel 4 Bit 2 (Channel 4 Channel Enable)
CSR[4][1] - Channel 4 Bit 1 (Channel 4 Synchronous Reset)
CSR[4][0] - Channel 4 Bit 0 (Channel 4 Clock Enable)

CSR[5][3] - Channel 5 Bit 3 (Channel 5 Output Enable)
CSR[5][2] - Channel 5 Bit 2 (Channel 5 Channel Enable)
CSR[5][1] - Channel 5 Bit 1 (Channel 5 Synchronous Reset)
CSR[5][0] - Channel 5 Bit 0 (Channel 5 Clock Enable)

CSR[6][3] - Channel 6 Bit 3 (Channel 6 Output Enable)
CSR[6][2] - Channel 6 Bit 2 (Channel 6 Channel Enable)
CSR[6][1] - Channel 6 Bit 1 (Channel 6 Synchronous Reset)
CSR[6][0] - Channel 6 Bit 0 (Channel 6 Clock Enable)

CSR[7][3] - Channel 7 Bit 3 (Channel 7 Output Enable)
CSR[7][2] - Channel 7 Bit 2 (Channel 7 Channel Enable)
CSR[7][1] - Channel 7 Bit 1 (Channel 7 Synchronous Reset)
CSR[7][0] - Channel 7 Bit 0 (Channel 7 Clock Enable)

Register Definitions - Control and Status Registers

CSR[15:0][3:0] - 16 Channel 4 Bit Control and Status Register

CSR[8][3] - Channel 8 Bit 3 (Channel 8 Output Enable)
CSR[8][2] - Channel 8 Bit 2 (Channel 8 Channel Enable)
CSR[8][1] - Channel 8 Bit 1 (Channel 8 Synchronous Reset)
CSR[8][0] - Channel 8 Bit 0 (Channel 8 Clock Enable)

CSR[9][3] - Channel 9 Bit 3 (Channel 9 Output Enable)
CSR[9][2] - Channel 9 Bit 2 (Channel 9 Channel Enable)
CSR[9][1] - Channel 9 Bit 1 (Channel 9 Synchronous Reset)
CSR[9][0] - Channel 9 Bit 0 (Channel 9 Clock Enable)

CSR[10][3] - Channel 10 Bit 3 (Channel 10 Output Enable)
CSR[10][2] - Channel 10 Bit 2 (Channel 10 Channel Enable)
CSR[10][1] - Channel 10 Bit 1 (Channel 10 Synchronous Reset)
CSR[10][0] - Channel 10 Bit 0 (Channel 10 Clock Enable)

CSR[11][3] - Channel 11 Bit 3 (Channel 11 Output Enable)
CSR[11][2] - Channel 11 Bit 2 (Channel 11 Channel Enable)
CSR[11][1] - Channel 11 Bit 1 (Channel 11 Synchronous Reset)
CSR[11][0] - Channel 11 Bit 0 (Channel 11 Clock Enable)

CSR[12][3] - Channel 12 Bit 3 (Channel 12 Output Enable)
CSR[12][2] - Channel 12 Bit 2 (Channel 12 Channel Enable)
CSR[12][1] - Channel 12 Bit 1 (Channel 12 Synchronous Reset)
CSR[12][0] - Channel 12 Bit 0 (Channel 12 Clock Enable)

CSR[13][3] - Channel 13 Bit 3 (Channel 13 Output Enable)
CSR[13][2] - Channel 13 Bit 2 (Channel 13 Channel Enable)
CSR[13][1] - Channel 13 Bit 1 (Channel 13 Synchronous Reset)
CSR[13][0] - Channel 13 Bit 0 (Channel 13 Clock Enable)

CSR[14][3] - Channel 14 Bit 3 (Channel 14 Output Enable)
CSR[14][2] - Channel 14 Bit 2 (Channel 14 Channel Enable)
CSR[14][1] - Channel 14 Bit 1 (Channel 14 Synchronous Reset)
CSR[14][0] - Channel 14 Bit 0 (Channel 14 Clock Enable)

CSR[15][3] - Channel 15 Bit 3 (Channel 15 Output Enable)
CSR[15][2] - Channel 15 Bit 2 (Channel 15 Channel Enable)
CSR[15][1] - Channel 15 Bit 1 (Channel 15 Synchronous Reset)
CSR[15][0] - Channel 15 Bit 0 (Channel 15 Clock Enable)

Register Definitions - Psudeo Noise (PN) Sequence Registers

PN0[0][4]	-	Register 0 / Channel 0 / Bit 4
PN0[0][3]	-	Register 0 / Channel 0 / Bit 3
PN0[0][2]	-	Register 0 / Channel 0 / Bit 2
PN0[0][1]	-	Register 0 / Channel 0 / Bit 1
PN0[0][0]	-	Register 0 / Channel 0 / Bit 0
PN0[1][4]	-	Register 0 / Channel 1 / Bit 4
PN0[1][3]	-	Register 0 / Channel 1 / Bit 3
PN0[1][2]	-	Register 0 / Channel 1 / Bit 2
PN0[1][1]	-	Register 0 / Channel 1 / Bit 1
PN0[1][0]	-	Register 0 / Channel 1 / Bit 0
PN0[2][4]	-	Register 0 / Channel 2 / Bit 4
PN0[2][3]	-	Register 0 / Channel 2 / Bit 3
PN0[2][2]	-	Register 0 / Channel 2 / Bit 2
PN0[2][1]	-	Register 0 / Channel 2 / Bit 1
PN0[2][0]	-	Register 0 / Channel 2 / Bit 0
PN0[3][4]	-	Register 0 / Channel 3 / Bit 4
PN0[3][3]	-	Register 0 / Channel 3 / Bit 3
PN0[3][2]	-	Register 0 / Channel 3 / Bit 2
PN0[3][1]	-	Register 0 / Channel 3 / Bit 1
PN0[3][0]	-	Register 0 / Channel 3 / Bit 0
PN0[4][4]	-	Register 0 / Channel 4 / Bit 4
PN0[4][3]	-	Register 0 / Channel 4 / Bit 3
PN0[4][2]	-	Register 0 / Channel 4 / Bit 2
PN0[4][1]	-	Register 0 / Channel 4 / Bit 1
PN0[4][0]	-	Register 0 / Channel 4 / Bit 0
PN0[5][4]	-	Register 0 / Channel 5 / Bit 4
PN0[5][3]	-	Register 0 / Channel 5 / Bit 3
PN0[5][2]	-	Register 0 / Channel 5 / Bit 2
PN0[5][1]	-	Register 0 / Channel 5 / Bit 1
PN0[5][0]	-	Register 0 / Channel 5 / Bit 0

Register Definitions - Psudeo Noise (PN) Sequence Registers

PN0[6][4]	-	Register 0 / Channel 6 / Bit 4
PN0[6][3]	-	Register 0 / Channel 6 / Bit 3
PN0[6][2]	-	Register 0 / Channel 6 / Bit 2
PN0[6][1]	-	Register 0 / Channel 6 / Bit 1
PN0[6][0]	-	Register 0 / Channel 6 / Bit 0
PN0[7][4]	-	Register 0 / Channel 7 / Bit 4
PN0[7][3]	-	Register 0 / Channel 7 / Bit 3
PN0[7][2]	-	Register 0 / Channel 7 / Bit 2
PN0[7][1]	-	Register 0 / Channel 7 / Bit 1
PN0[7][0]	-	Register 0 / Channel 7 / Bit 0
PN0[8][4]	-	Register 0 / Channel 8 / Bit 4
PN0[8][3]	-	Register 0 / Channel 8 / Bit 3
PN0[8][2]	-	Register 0 / Channel 8 / Bit 2
PN0[8][1]	-	Register 0 / Channel 8 / Bit 1
PN0[8][0]	-	Register 0 / Channel 8 / Bit 0
PN0[9][4]	-	Register 0 / Channel 9 / Bit 4
PN0[9][3]	-	Register 0 / Channel 9 / Bit 3
PN0[9][2]	-	Register 0 / Channel 9 / Bit 2
PN0[9][1]	-	Register 0 / Channel 9 / Bit 1
PN0[9][0]	-	Register 0 / Channel 9 / Bit 0
PN0[10][4]	-	Register 0 / Channel 10 / Bit 4
PN0[10][3]	-	Register 0 / Channel 10 / Bit 3
PN0[10][2]	-	Register 0 / Channel 10 / Bit 2
PN0[10][1]	-	Register 0 / Channel 10 / Bit 1
PN0[10][0]	-	Register 0 / Channel 10 / Bit 0
PN0[11][4]	-	Register 0 / Channel 11 / Bit 4
PN0[11][3]	-	Register 0 / Channel 11 / Bit 3
PN0[11][2]	-	Register 0 / Channel 11 / Bit 2
PN0[11][1]	-	Register 0 / Channel 11 / Bit 1
PN0[11][0]	-	Register 0 / Channel 11 / Bit 0

Register Definitions - Psudeo Noise (PN) Sequence Register

PN0[12][4]	-	Register 0 / Channel 12 / Bit 4
PN0[12][3]	-	Register 0 / Channel 12 / Bit 3
PN0[12][2]	-	Register 0 / Channel 12 / Bit 2
PN0[12][1]	-	Register 0 / Channel 12 / Bit 1
PN0[12][0]	-	Register 0 / Channel 12 / Bit 0
PN0[13][4]	-	Register 0 / Channel 13 / Bit 4
PN0[13][3]	-	Register 0 / Channel 13 / Bit 3
PN0[13][2]	-	Register 0 / Channel 13 / Bit 2
PN0[13][1]	-	Register 0 / Channel 13 / Bit 1
PN0[13][0]	-	Register 0 / Channel 13 / Bit 0
PN0[14][4]	-	Register 0 / Channel 14 / Bit 4
PN0[14][3]	-	Register 0 / Channel 14 / Bit 3
PN0[14][2]	-	Register 0 / Channel 14 / Bit 2
PN0[14][1]	-	Register 0 / Channel 14 / Bit 1
PN0[14][0]	-	Register 0 / Channel 14 / Bit 0
PN0[15][4]	-	Register 0 / Channel 15 / Bit 4
PN0[15][3]	-	Register 0 / Channel 15 / Bit 3
PN0[15][2]	-	Register 0 / Channel 15 / Bit 2
PN0[15][1]	-	Register 0 / Channel 15 / Bit 1
PN0[15][0]	-	Register 0 / Channel 15 / Bit 0
PN1[0][4]	-	Register 1 / Channel 0 / Bit 4
PN1[0][3]	-	Register 1 / Channel 0 / Bit 3
PN1[0][2]	-	Register 1 / Channel 0 / Bit 2
PN1[0][1]	-	Register 1 / Channel 0 / Bit 1
PN1[0][0]	-	Register 1 / Channel 0 / Bit 0
PN1[1][4]	-	Register 1 / Channel 1 / Bit 4
PN1[1][3]	-	Register 1 / Channel 1 / Bit 3
PN1[1][2]	-	Register 1 / Channel 1 / Bit 2
PN1[1][1]	-	Register 1 / Channel 1 / Bit 1
PN1[1][0]	-	Register 1 / Channel 1 / Bit 0

Register Definitions - Psudeo Noise (PN) Sequence Registers

PN1[2][4]	-	Register 1 / Channel 2 / Bit 4
PN1[2][3]	-	Register 1 / Channel 2 / Bit 3
PN1[2][2]	-	Register 1 / Channel 2 / Bit 2
PN1[2][1]	-	Register 1 / Channel 2 / Bit 1
PN1[2][0]	-	Register 1 / Channel 2 / Bit 0
PN1[3][4]	-	Register 1 / Channel 3 / Bit 4
PN1[3][3]	-	Register 1 / Channel 3 / Bit 3
PN1[3][2]	-	Register 1 / Channel 3 / Bit 2
PN1[3][1]	-	Register 1 / Channel 3 / Bit 1
PN1[3][0]	-	Register 1 / Channel 3 / Bit 0
PN1[4][4]	-	Register 1 / Channel 4 / Bit 4
PN1[4][3]	-	Register 1 / Channel 4 / Bit 3
PN1[4][2]	-	Register 1 / Channel 4 / Bit 2
PN1[4][1]	-	Register 1 / Channel 4 / Bit 1
PN1[4][0]	-	Register 1 / Channel 4 / Bit 0
PN1[5][4]	-	Register 1 / Channel 5 / Bit 4
PN1[5][3]	-	Register 1 / Channel 5 / Bit 3
PN1[5][2]	-	Register 1 / Channel 5 / Bit 2
PN1[5][1]	-	Register 1 / Channel 5 / Bit 1
PN1[5][0]	-	Register 1 / Channel 5 / Bit 0
PN1[6][4]	-	Register 1 / Channel 6 / Bit 4
PN1[6][3]	-	Register 1 / Channel 6 / Bit 3
PN1[6][2]	-	Register 1 / Channel 6 / Bit 2
PN1[6][1]	-	Register 1 / Channel 6 / Bit 1
PN1[6][0]	-	Register 1 / Channel 6 / Bit 0
PN1[7][4]	-	Register 1 / Channel 7 / Bit 4
PN1[7][3]	-	Register 1 / Channel 7 / Bit 3
PN1[7][2]	-	Register 1 / Channel 7 / Bit 2
PN1[7][1]	-	Register 1 / Channel 7 / Bit 1
PN1[7][0]	-	Register 1 / Channel 7 / Bit 0

Register Definitions - Psudeo Noise (PN) Sequence Registers

PN1[8][4]	-	Register 1 / Channel 8 / Bit 4
PN1[8][3]	-	Register 1 / Channel 8 / Bit 3
PN1[8][2]	-	Register 1 / Channel 8 / Bit 2
PN1[8][1]	-	Register 1 / Channel 8 / Bit 1
PN1[8][0]	-	Register 1 / Channel 8 / Bit 0
PN1[9][4]	-	Register 1 / Channel 9 / Bit 4
PN1[9][3]	-	Register 1 / Channel 9 / Bit 3
PN1[9][2]	-	Register 1 / Channel 9 / Bit 2
PN1[9][1]	-	Register 1 / Channel 9 / Bit 1
PN1[9][0]	-	Register 1 / Channel 9 / Bit 0
PN1[10][4]	-	Register 1 / Channel 10 / Bit 4
PN1[10][3]	-	Register 1 / Channel 10 / Bit 3
PN1[10][2]	-	Register 1 / Channel 10 / Bit 2
PN1[10][1]	-	Register 1 / Channel 10 / Bit 1
PN1[10][0]	-	Register 1 / Channel 10 / Bit 0
PN1[11][4]	-	Register 1 / Channel 11 / Bit 4
PN1[11][3]	-	Register 1 / Channel 11 / Bit 3
PN1[11][2]	-	Register 1 / Channel 11 / Bit 2
PN1[11][1]	-	Register 1 / Channel 11 / Bit 1
PN1[11][0]	-	Register 1 / Channel 11 / Bit 0
PN1[12][4]	-	Register 1 / Channel 12 / Bit 4
PN1[12][3]	-	Register 1 / Channel 12 / Bit 3
PN1[12][2]	-	Register 1 / Channel 12 / Bit 2
PN1[12][1]	-	Register 1 / Channel 12 / Bit 1
PN1[12][0]	-	Register 1 / Channel 12 / Bit 0
PN1[13][4]	-	Register 1 / Channel 13 / Bit 4
PN1[13][3]	-	Register 1 / Channel 13 / Bit 3
PN1[13][2]	-	Register 1 / Channel 13 / Bit 2
PN1[13][1]	-	Register 1 / Channel 13 / Bit 1
PN1[13][0]	-	Register 1 / Channel 13 / Bit 0

Register Definitions - Psudeo Noise (PN) Sequence Registers

PN1[14][4]	-	Register 1 / Channel 14 / Bit 4
PN1[14][3]	-	Register 1 / Channel 14 / Bit 3
PN1[14][2]	-	Register 1 / Channel 14 / Bit 2
PN1[14][1]	-	Register 1 / Channel 14 / Bit 1
PN1[14][0]	-	Register 1 / Channel 14 / Bit 0
PN1[15][4]	-	Register 1 / Channel 15 / Bit 4
PN1[15][3]	-	Register 1 / Channel 15 / Bit 3
PN1[15][2]	-	Register 1 / Channel 15 / Bit 2
PN1[15][1]	-	Register 1 / Channel 15 / Bit 1
PN1[15][0]	-	Register 1 / Channel 15 / Bit 0

Register Definitions - Global Registers

OE	-	Global Output Enable
CE	-	Global Clock Enable

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

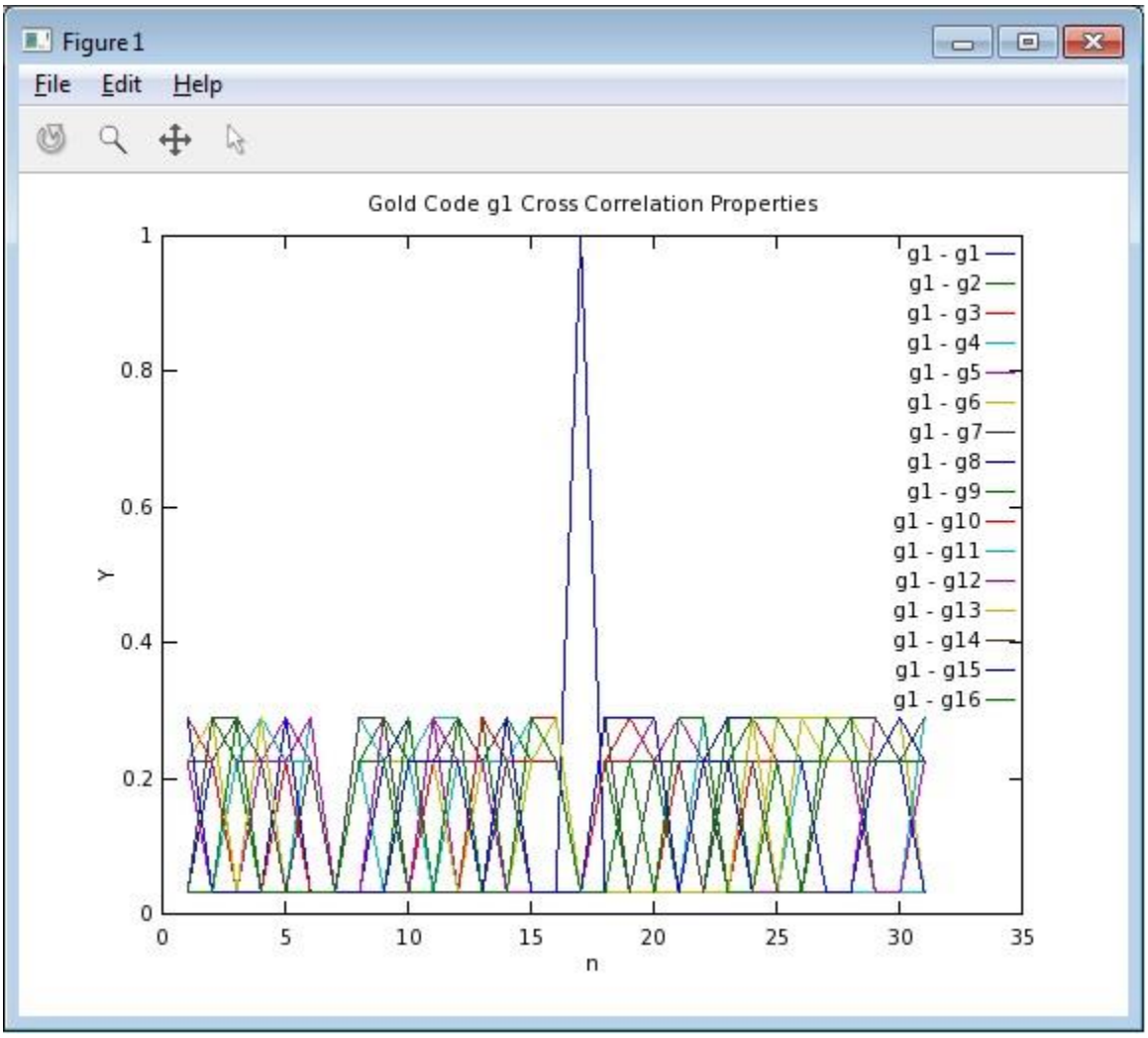

Figure 8: Gold Code g1 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

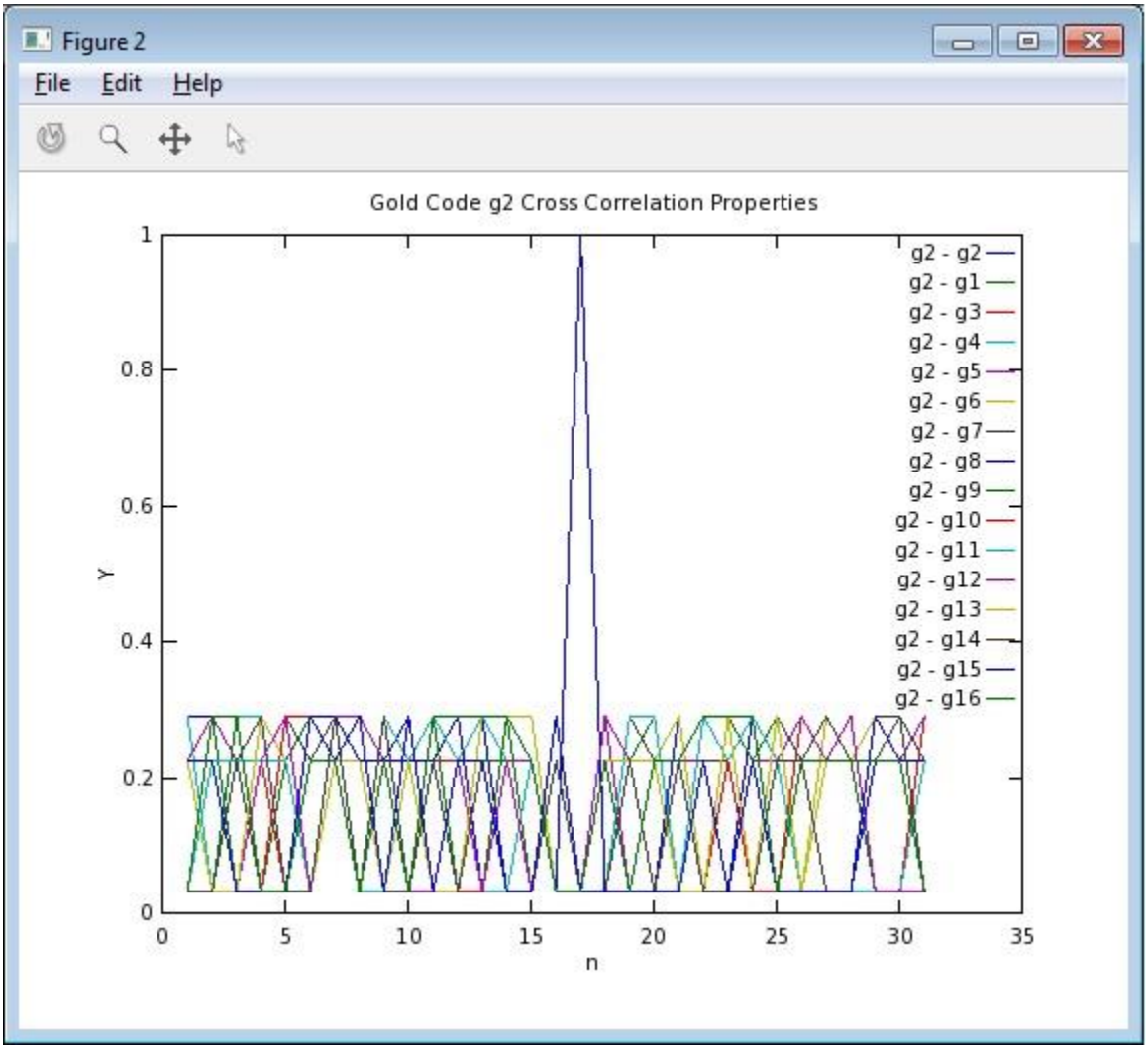

Figure 9: Gold Code g2 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

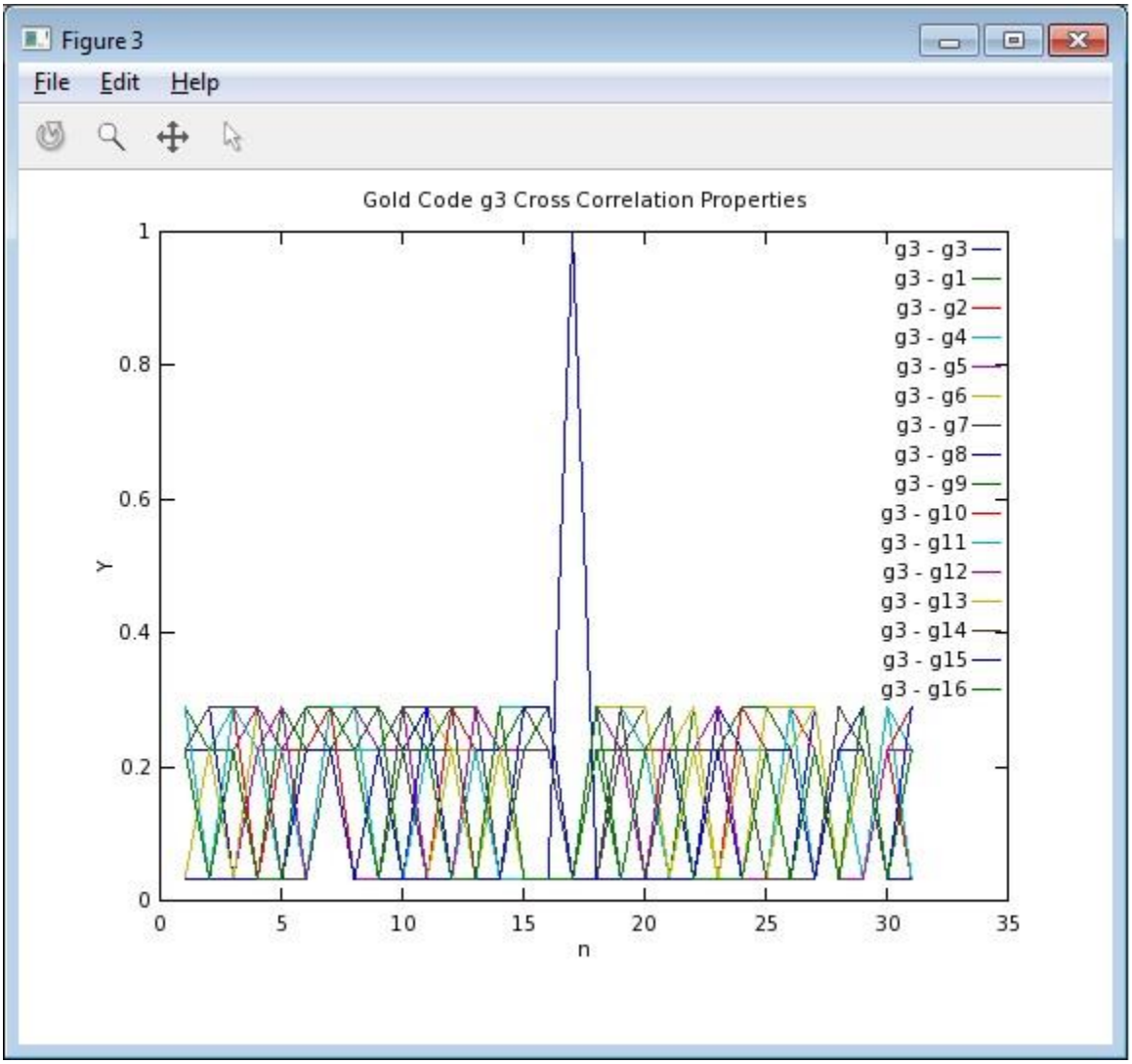

Figure 10: Gold Code g3 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

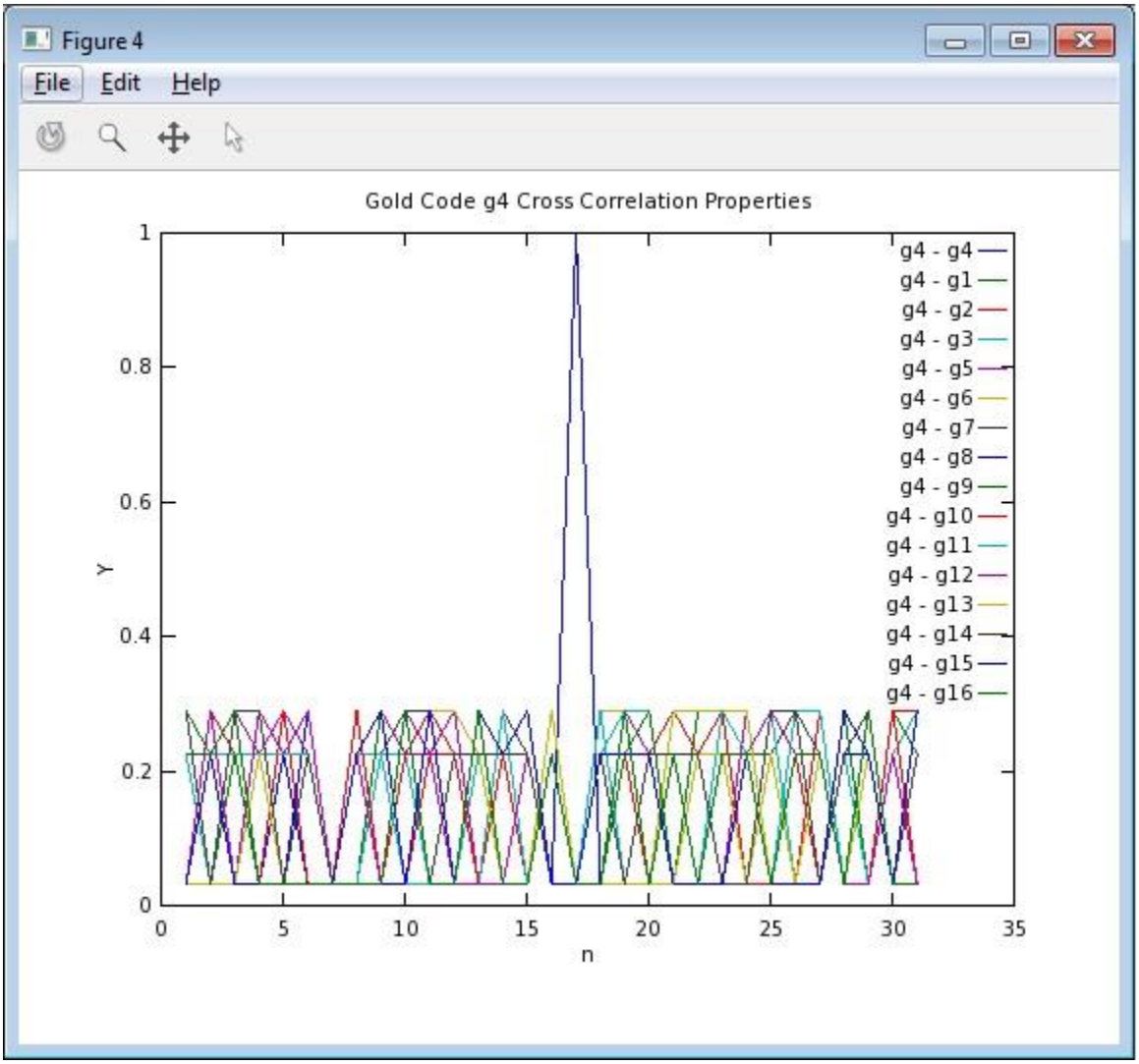

Figure 11: Gold Code g4 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

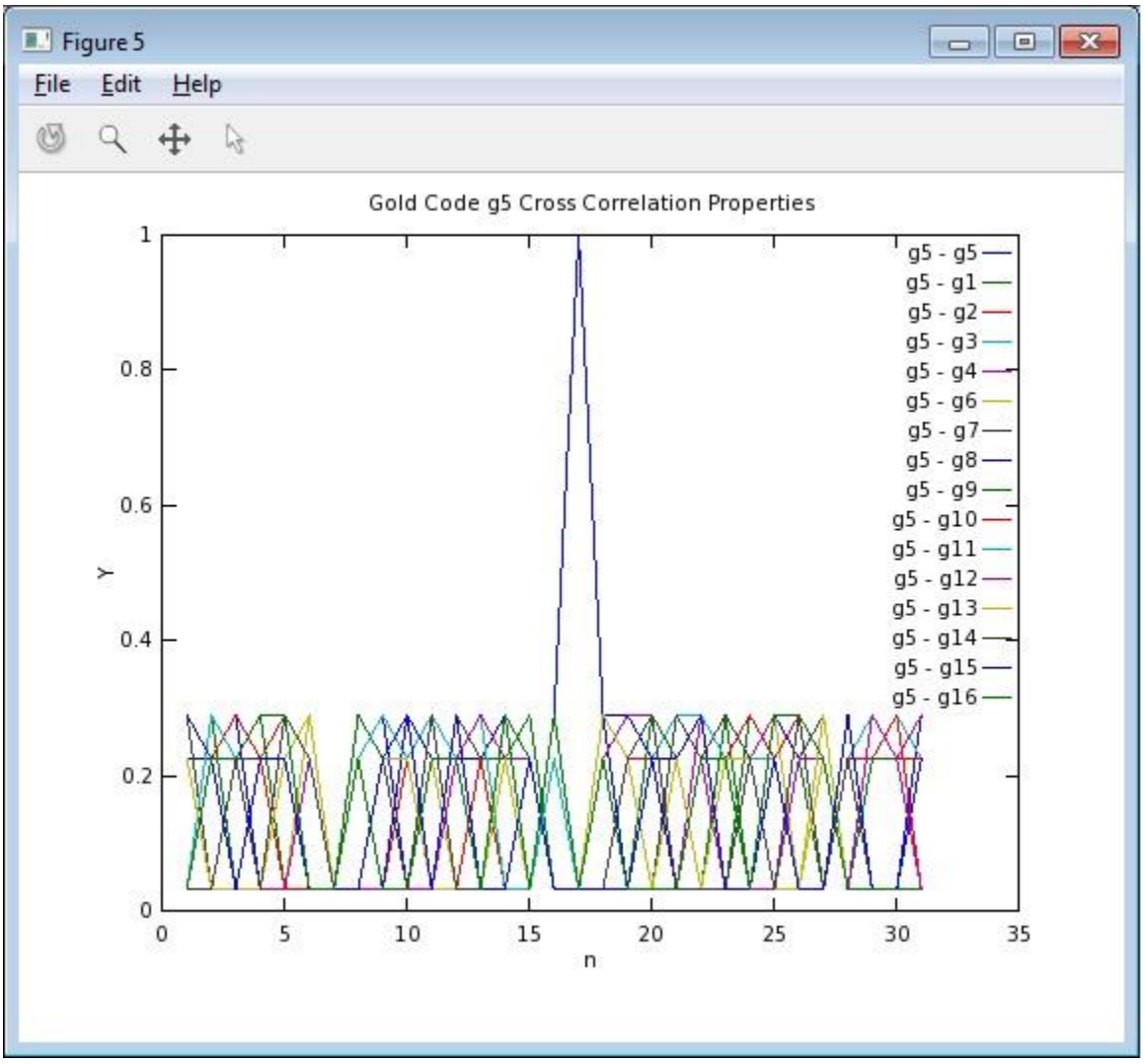

Figure 12: Gold Code g5 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

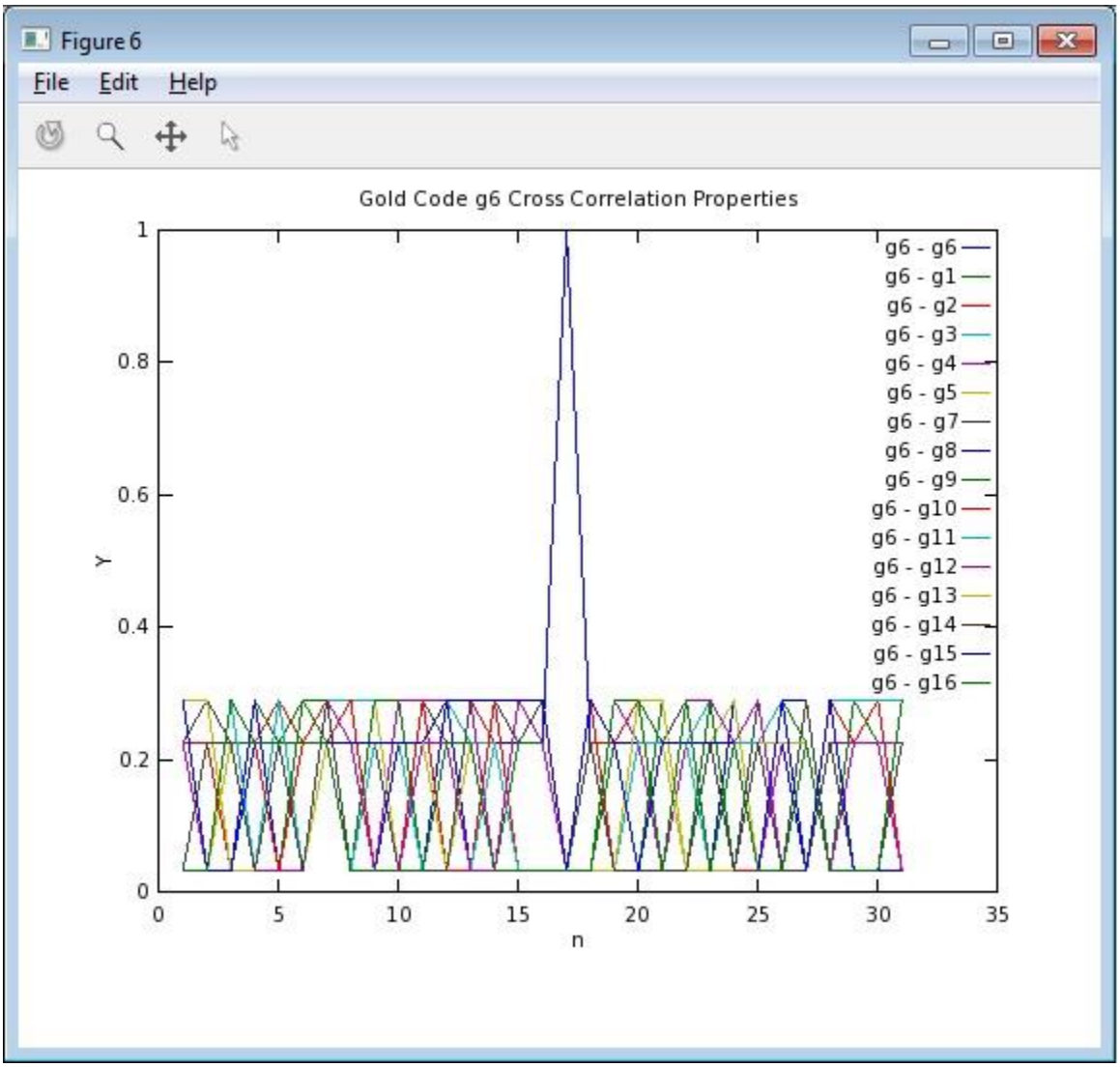

Figure 13: Gold Code g6 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

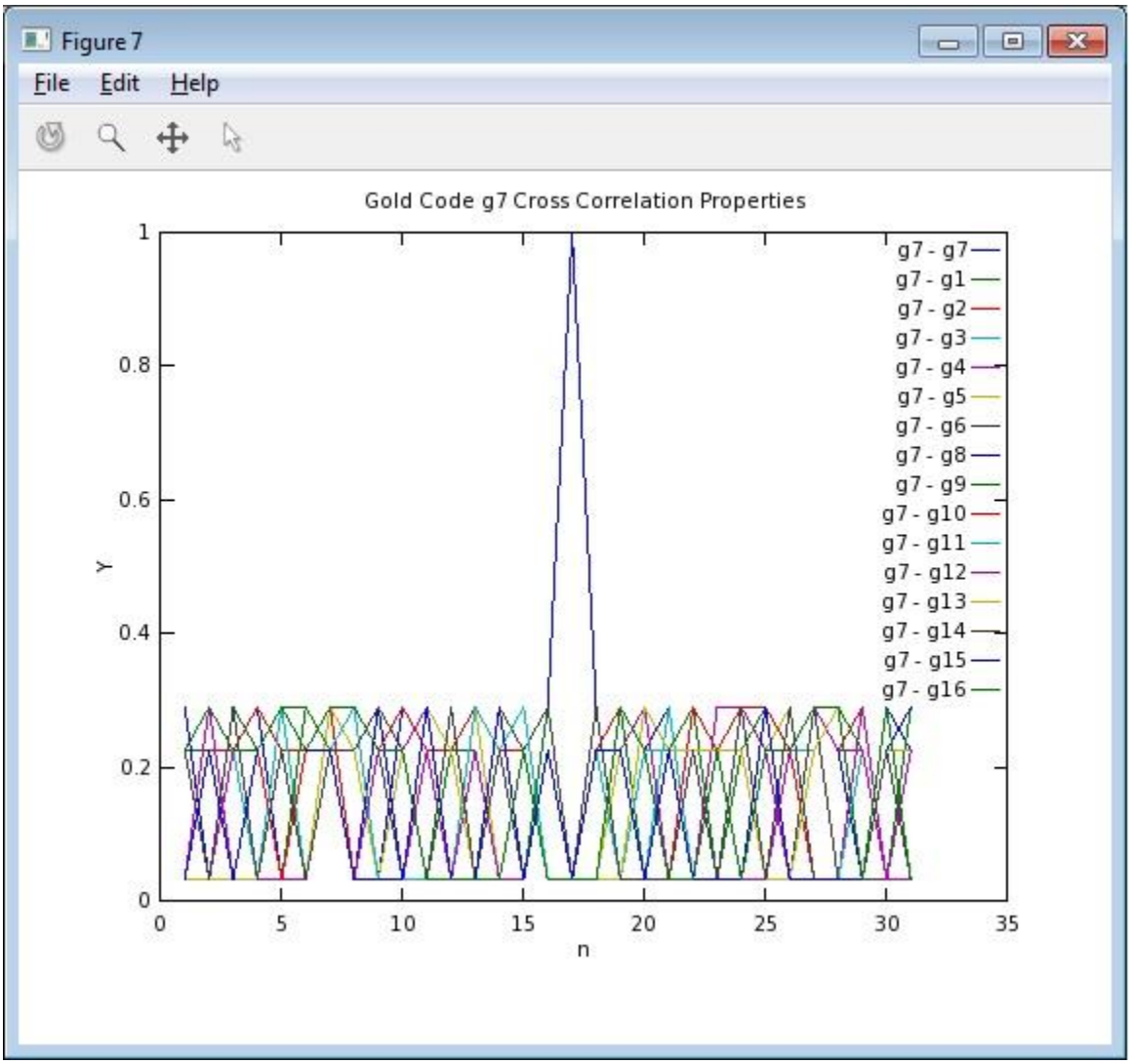

Figure 14: Gold Code g7 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

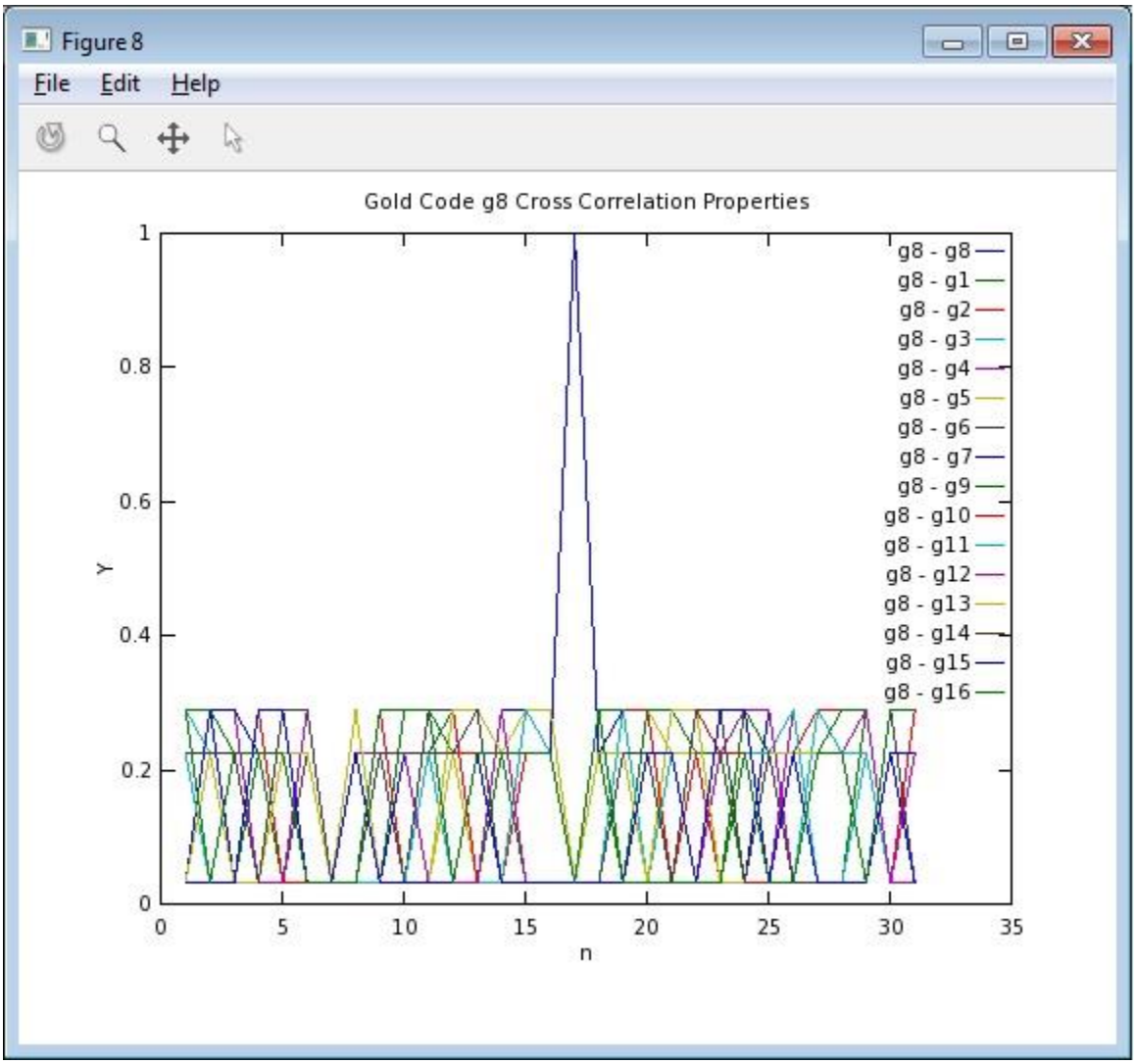

Figure 15: Gold Code g8 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

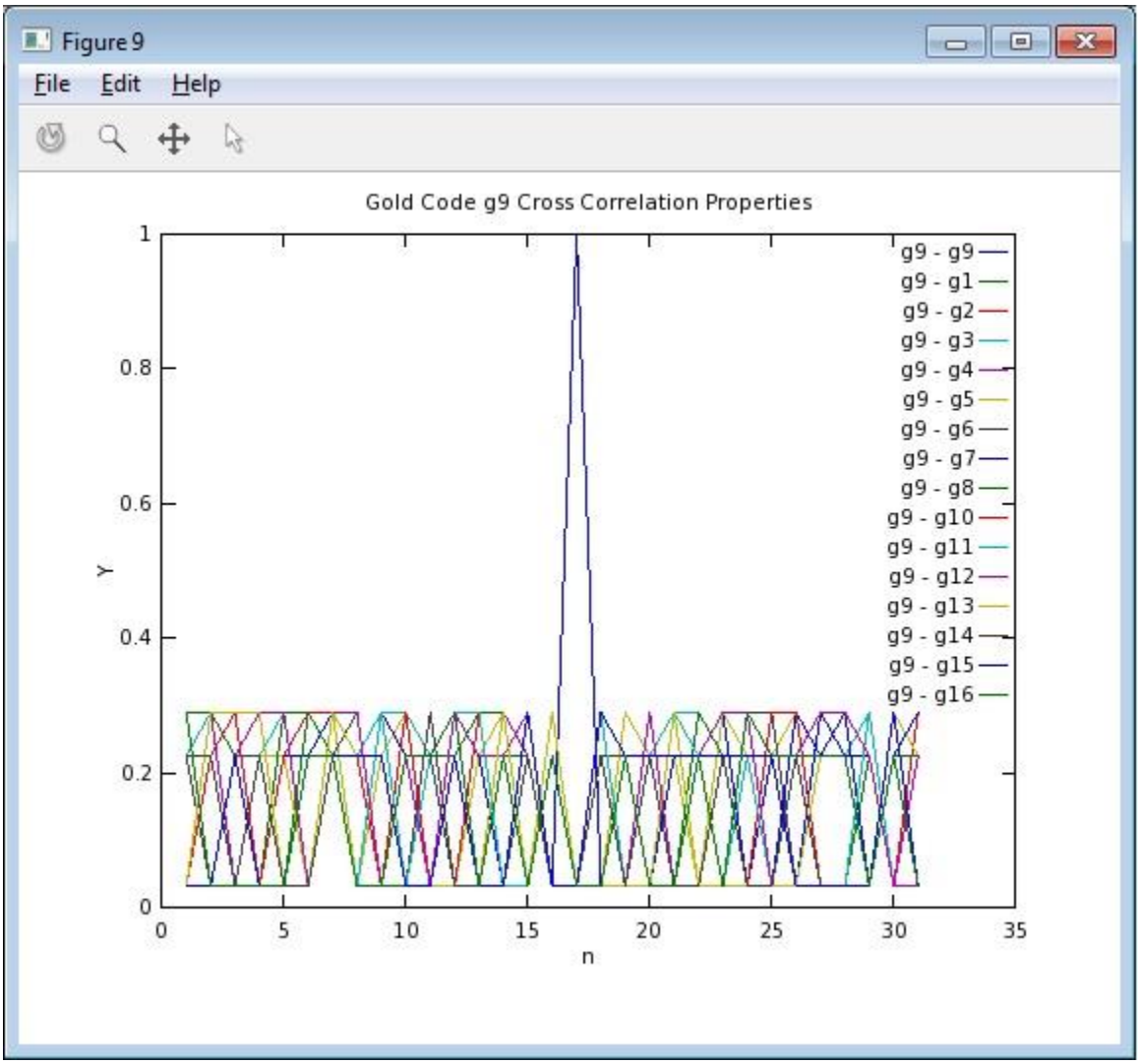

Figure 16: Gold Code g9 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

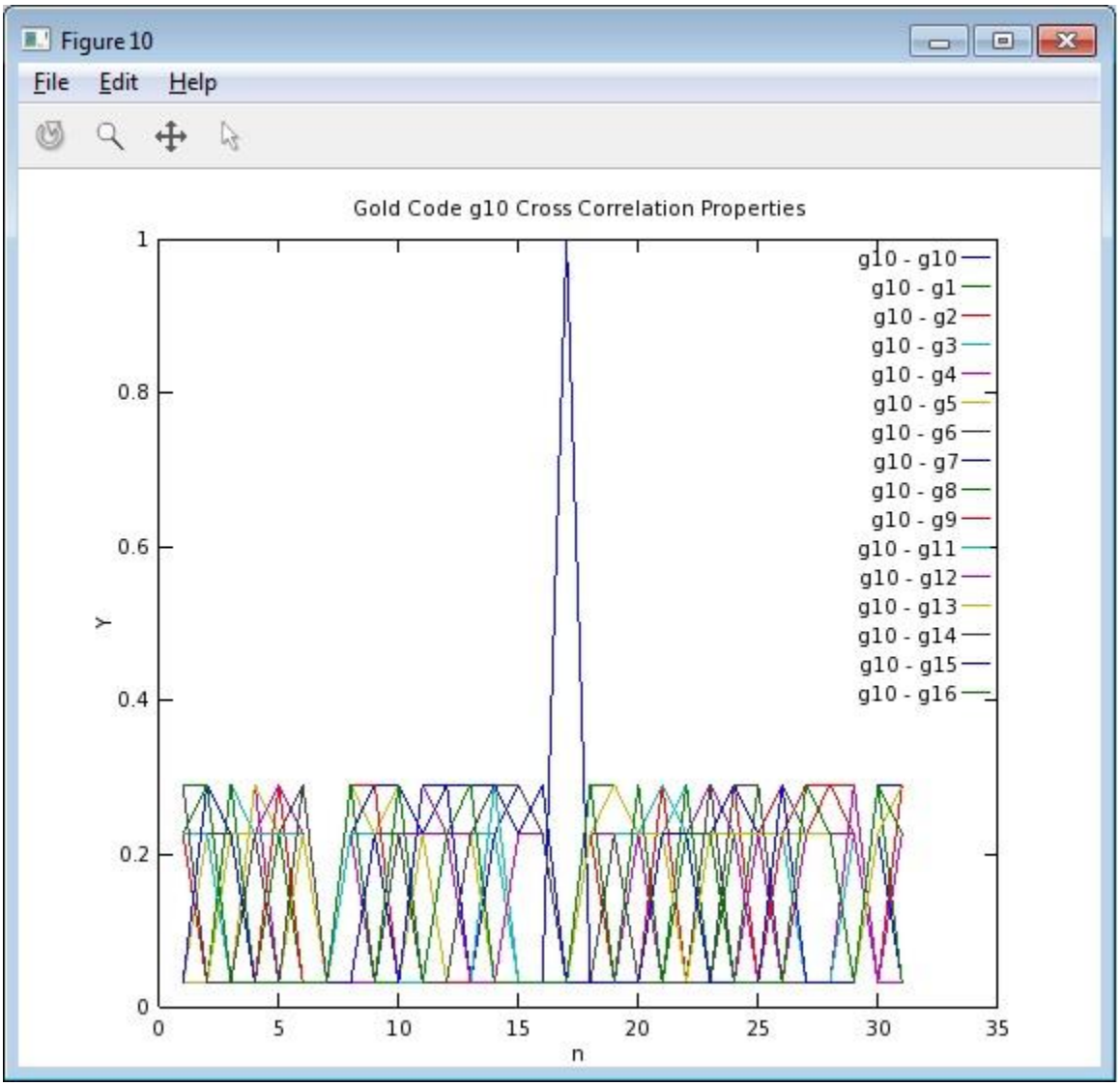

Figure 17: Gold Code g10 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

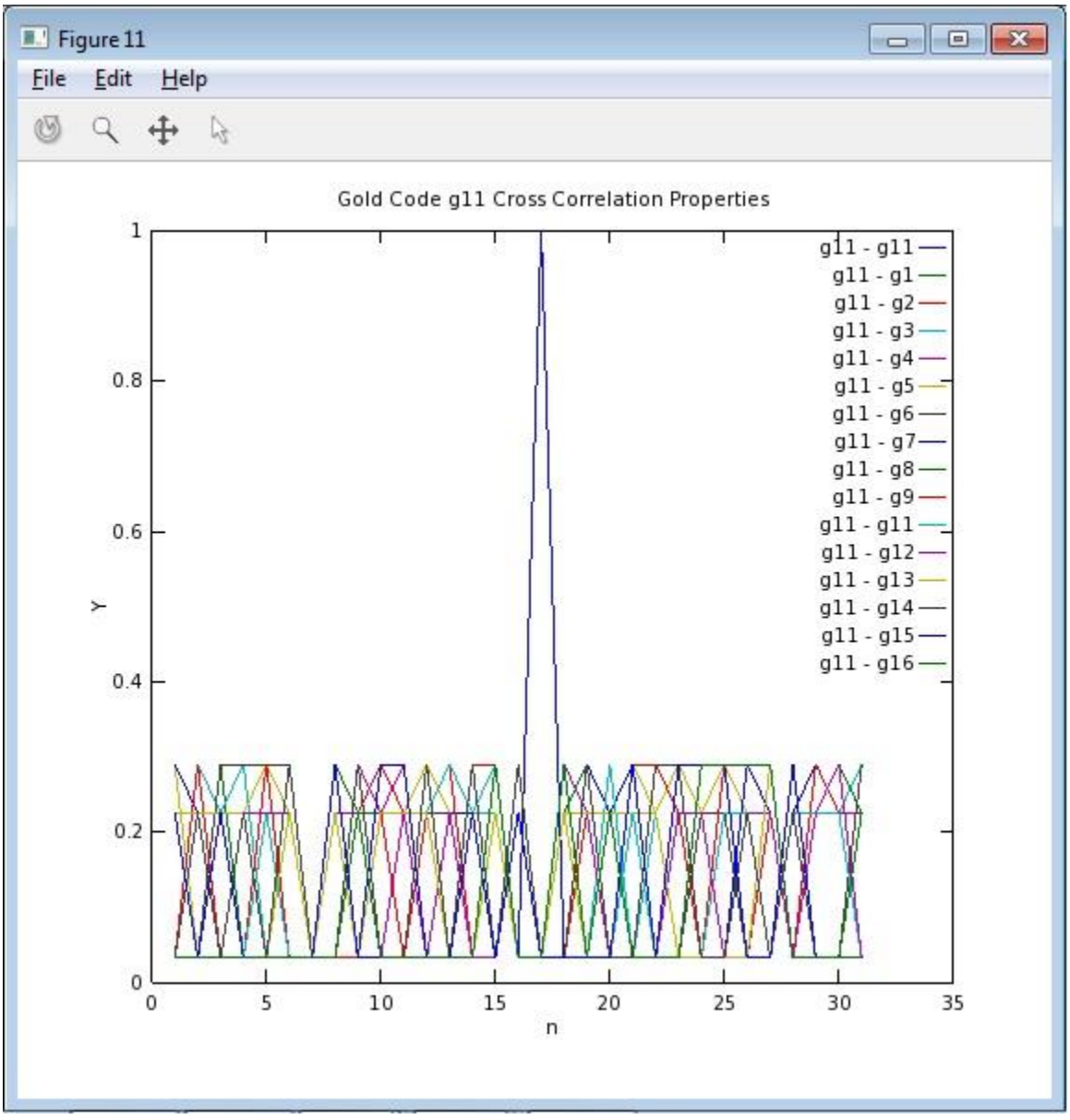

Figure 18: Gold Code g11 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

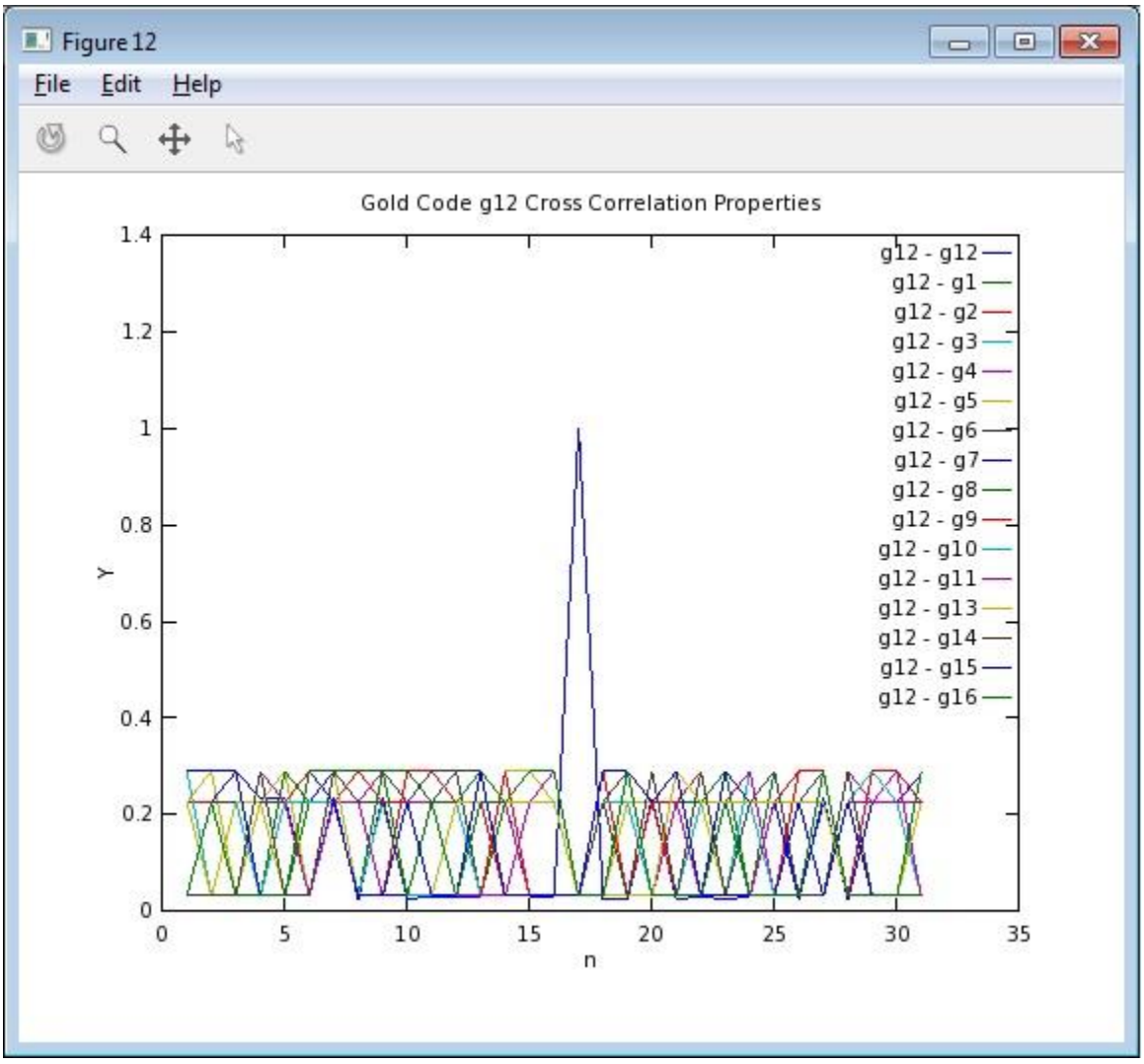

Figure 19: Gold Code g12 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

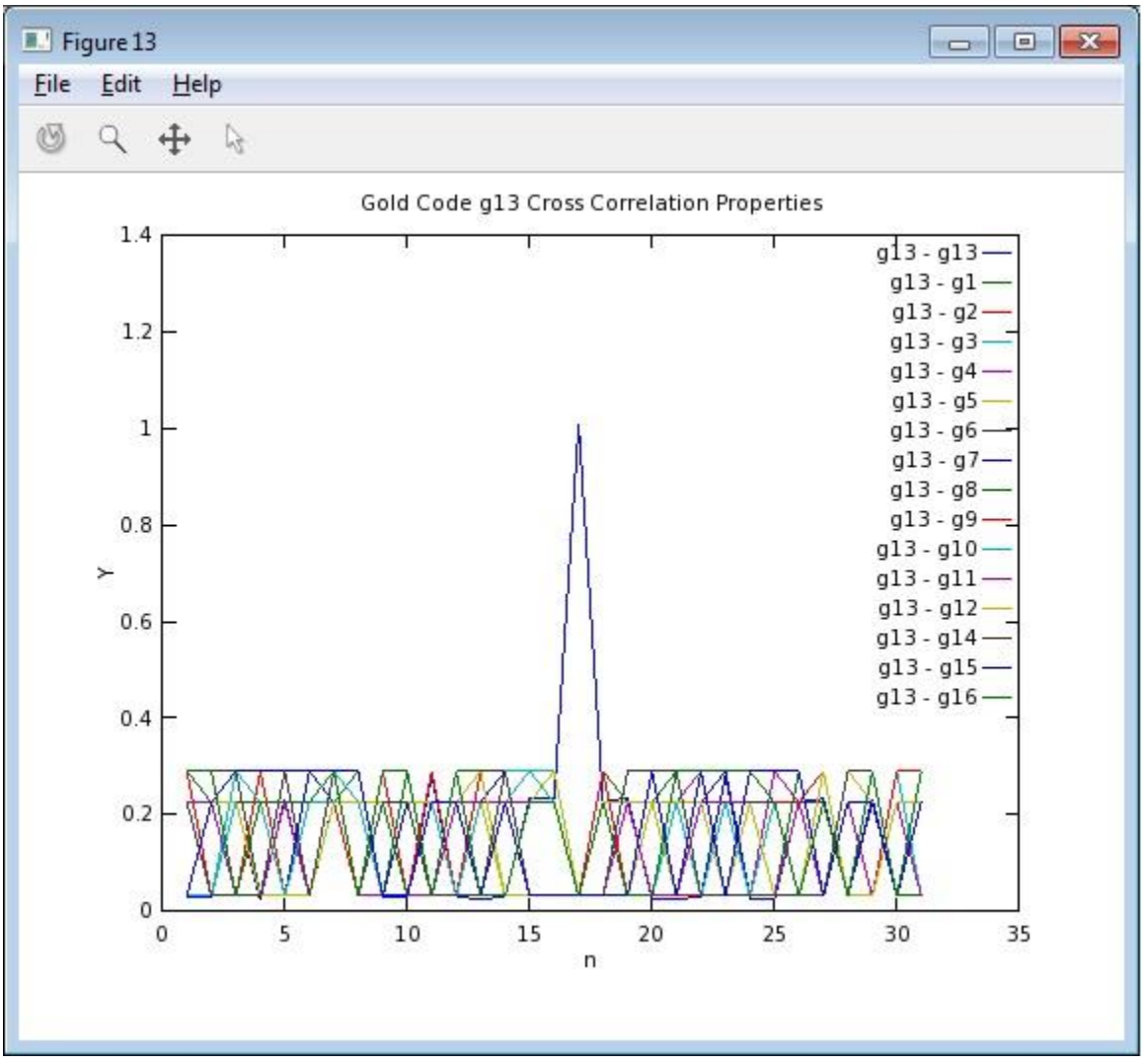

Figure 20: Gold Code g13 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

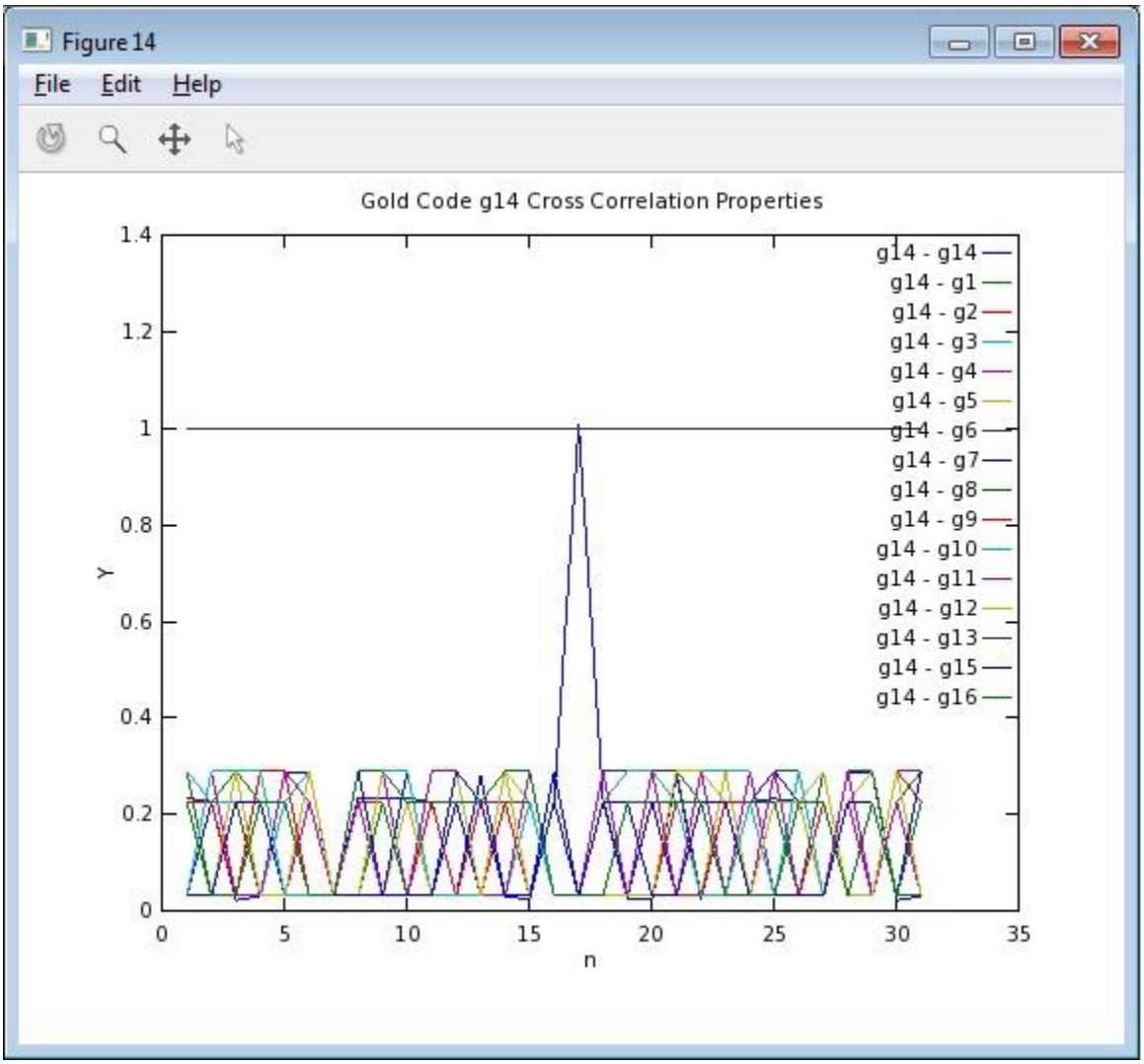

Figure 21: Gold Code g14 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

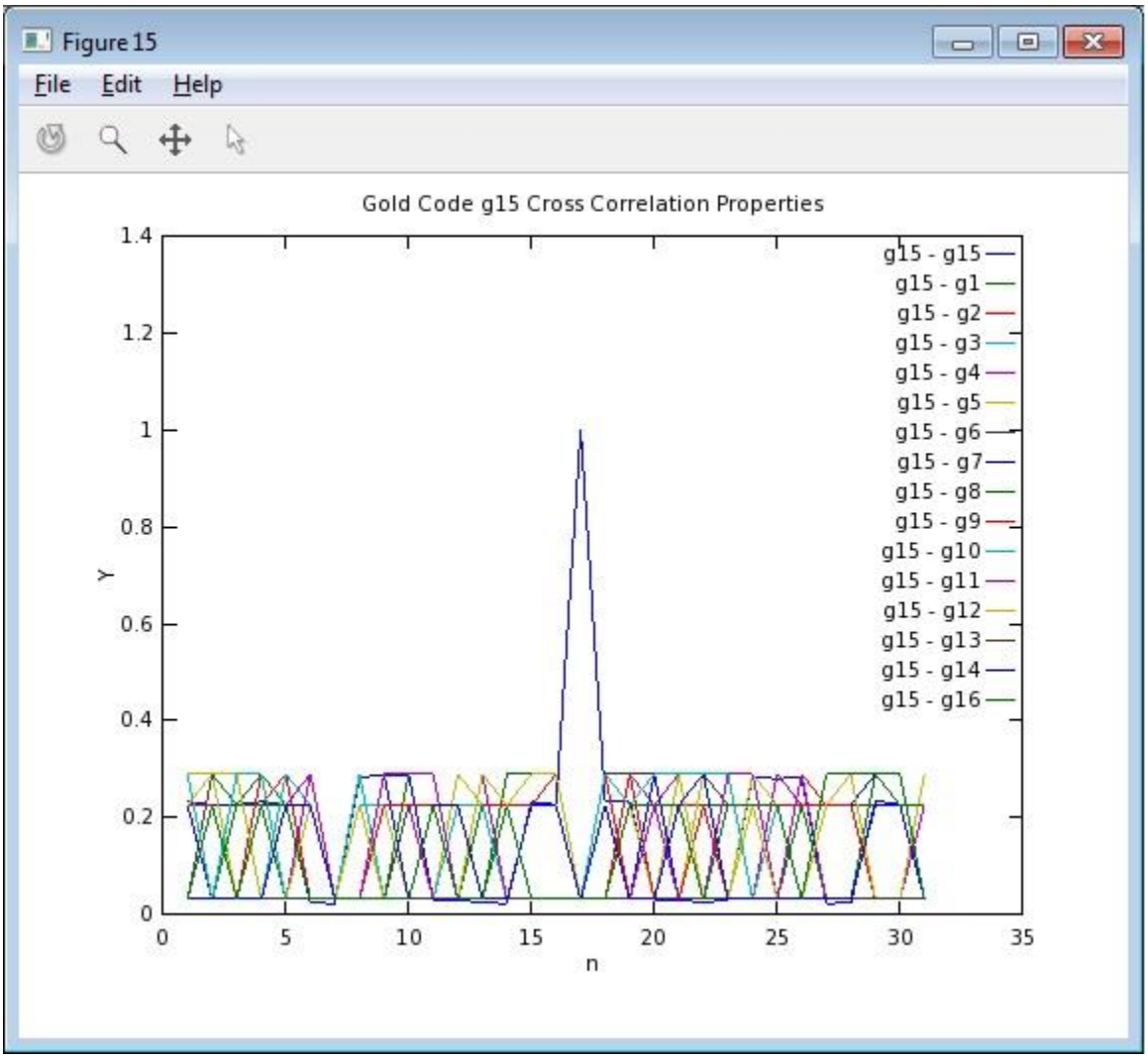

Figure 22: Gold Code g15 Cross Correlation Properties

Gold Code Technical Data – Cross Correlation

n = 5
Code Length = 31
16 Codes (g1 - g16)

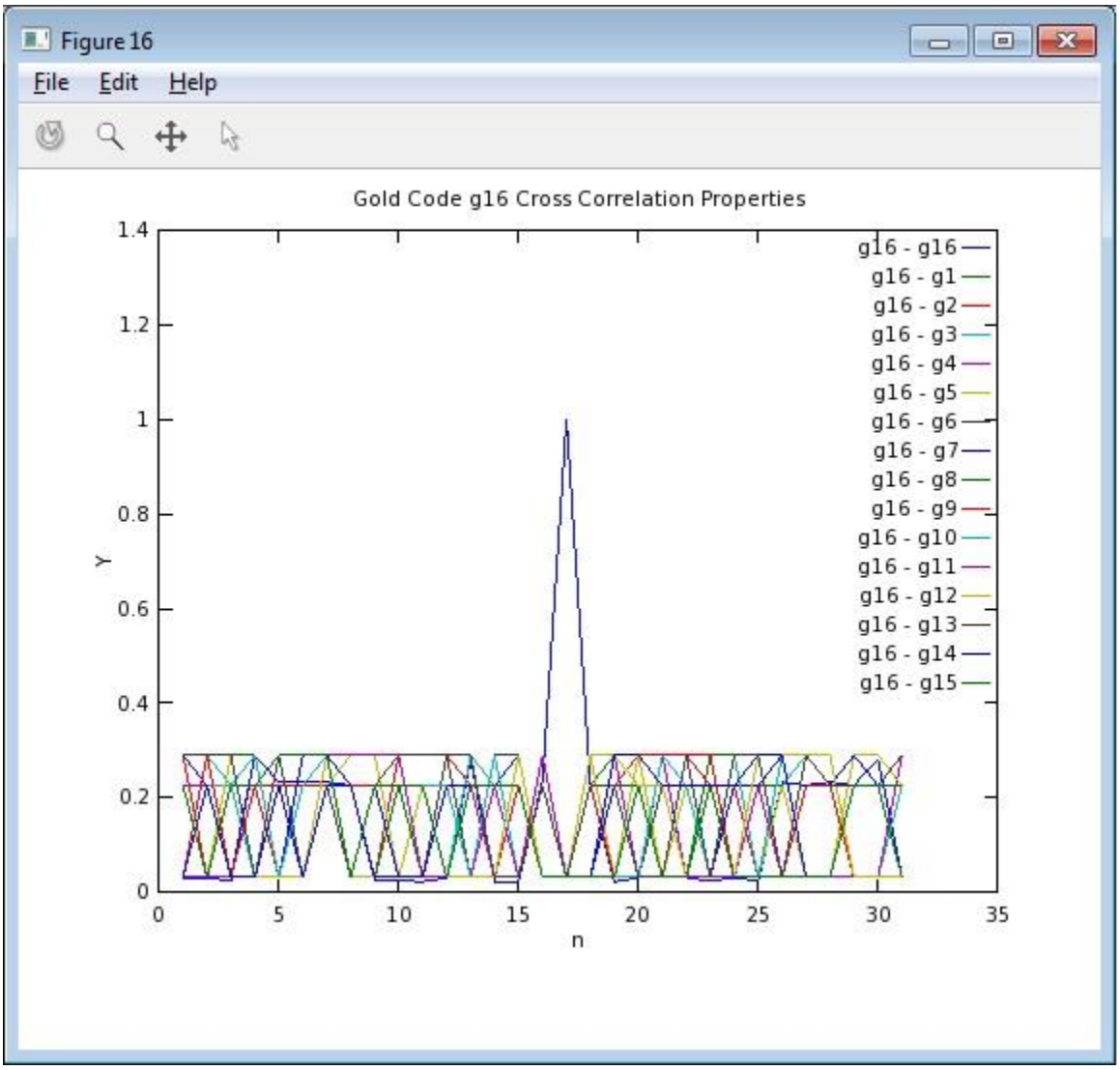

Figure 23: Gold Code g16 Cross Correlation Properties

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Preliminary Data Sheet

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